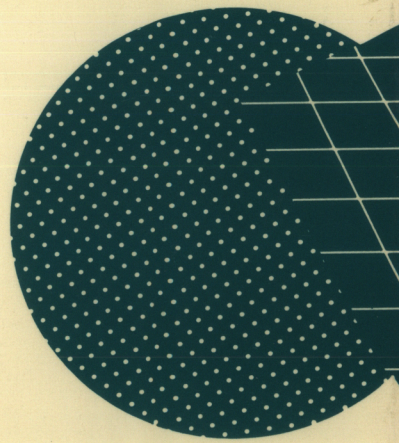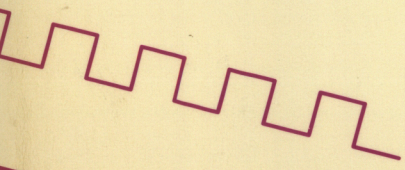# 1989 TELECOM PRODUCTS

DALLAS
SEMICONDUCTOR

SETTING DIGITAL COMMUNICATION TRENDS

Dallas Semiconductor has introduced chip sets that completely
support the T1,CEPT and ADPCM standards. In addition, we offer
subsystems called SipStiks™. These snap in subassemblies use JEDEC
standard configurations recently made popular by DRAMs.Their
low profile form factor achieves high functional density, yet offers
advantages of modularity.
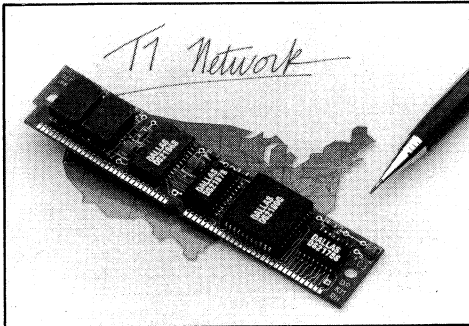
**North American or European
Short Loop Interface:**
The DS2280 and DS2281 are complete T1 and
CEPT Line Cards with transformers in less than 3
square inches. Both provide all of the interface
circuitry necessary for digital telephone networks.
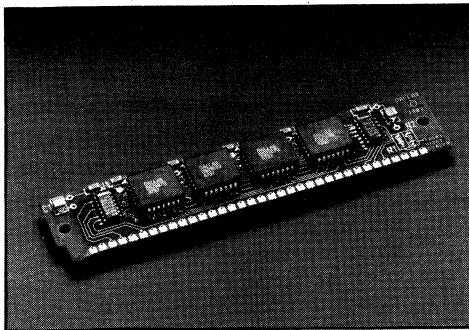
Multi-Channel Voice Compression:
The DS2264 and DS2268 offer 4 and 8 channel
ADPCM processing in the same compact format.
ADPCM increases the effective bandwidth of the
digital telephone network by compressing and
decompressing speech.

DALLAS
SEMICONDUCTOR   not the only name behind our products...

Quality Completes Our Innovation

Table of Contents

Dallas Semiconductor

General Information

General Information

Corporate Fact Sheet

Dallas Semiconductor designs, manufactures and markets CMOS integrated circuits using special Late Definition technology. Late Definition permits the exact definition of a product to be postponed until end use, thereby increasing flexibility.

PRODUCTS

Founded Febuary 1, 1984, Dallas Semiconductor has a multiproduct strategy to serve the needs of the computer and communications industry. Our optimism stems from the ability to sell "Soft Silicon" which can be readily tailored to solve the specific problems of our customers. Soft silicon results from the Late Definition technologies of lithium, laser , and implant. Lithium postpones definition until end use, thereby making the chip adaptive in the system. Laser postpones definition until just before the chip is placed in the package, and implant postpones definition until the last wafer process step.

LITHIUM

Advances in CMOS circuitry have reduced power requirements to the point that a chip,using appropriate circuitry, can be packaged with a miniature lithium energy source which will last the useful life of the equipment. This allows Dallas Semiconductor to make chips which don't forget. Our initial product offerings exploited this capability to make the much sought-after nonvolatile RAM. In November 1984 we began shipping 64K Nonvolatile SRAMs.

Keeping track of human time has not been an easy task for computers until our July 1985 announcement of the DS1216 SmartWatch. It precisely keeps calendar time down to the hundredth of a second,replacing what heretofore consumed a whole printed circuit board full of electronics. A lithium cell provides power for life.

The adaptive nature of CMOS/Lithium products is made evident by the April 1987 introduction of the DS5000 Soft Microcontroller. Designed with change in mind, it offers unprecedented software adaptability and crashproof operation. The capabilities of the Soft Microcontroller take it beyond mere update change and into the realm of learning. The DS5000 can capture a large amount of data in real time and remember it indefinitely. With the proper application software, the microcontroller can improve its performance based on that cumulative knowledge. July 1988 marked the shipment of the DS5000T Time Microcontroller, the first permanently powered microcontroller that logs events and schedules activities according to calendar time.

LASER

The laser creates uniqueness on a chip at low cost. A sub-micron positioning laser and formidable control software developed at Dallas can engrave individual chips with digital patterns making each one different. These after-the-fact changes to completed circuits give our laser-based products a competitive edge.

The first product that demonstrated our special laser technology was an extremely accurate time base, commonly referred to as a delay line. Before the August 1985 announcement date, it had only been possible to build such devices using a dozen components in a hybrid assembly. The DS1000 Silicon Delay Line series is a direct replacement tor hybrid delay lines which are widely used in conjunction with DRAMs and magnetic disks.

Other products use the laser to protect sensitive information and intellectual property by creating a powerful security mechanism in micro chips. The DS1204U Electronic Key is an example of a product which benefits from the laser in this regard. Exclusive blank Keys are defined by laser for each customer, adding to the overall security mechanism. Additional products are on the drawing board whereby the laser tailors the option content of the chip for a particular customer. In short, the laser lets Dallas Semiconductor define each chip uniquely after it is already operational. Difficult system problems have been solved by relying

on these special technologies, experience, and creativity, to offer our customers a more complete solution than the chip alone can provide. Often this requires a greater emphasis on packaging than traditional semiconductor producers have been accustomed. Sixty-five base products were put into production prior to October 1988, unified by our own CMOS technology.

MANUFACTURING AND FACILITIES

Dallas Semiconductor manufactures products at a 114,000 square-foot facility located at the company's headquarters in north Dallas. This location includes an advanced Class One wafer fabrication facility completed in 1987. Six-inch wafers are processed with circuits utilizing sub-micron geometries. Automated modular process technology provides substantial flexibility in the manufacturing process and significantly reduces the number of people required for operation, thereby decreasing manufacturing costs. The company's wafer fabrication facility contains a 10,000-square-foot cleanroom. The sensitivity of the manufacturing process to particulates and other contaminants requires a highly controlled, clean environment. All products are shipped from Dallas after final quality assurance testing.

MARKETING AND SALES

Dallas Semiconductor sells its products to a large and diverse customer base of both mature and emerging OEMs in the computer, telecommunications, instrumentation, and factory automation markets. The company coordinates its selling activity from its Dallas, Texas headquarters. Five area sales offices are staffed in Cherry Hill, New Jersey; Boca Raton, Florida; Cupertino, California; Los Angeles, California; Carmel, Indiana; and Birmingham, England. The Company's six area sales managers call on OEM accounts and coordinate the activities of 45 sales representative offices in North America and 22 in European countries and Asia. Dallas Semiconductor also markets its products in North America through a national stocking distributor and through ten regional distributors.

1

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Product Overview
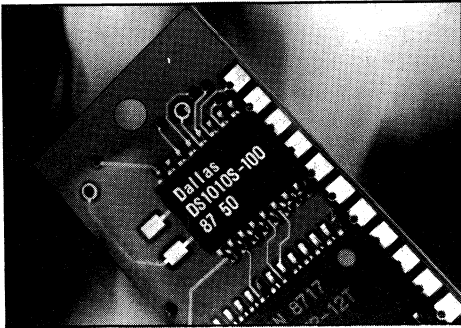
SILICON TIMED CIRCUITS

Electronic systems require exact timing to control the transmission of data between their component parts. Timing requirements vary across systems. Historically, systems designers have not been able to use semiconductors as timing references because of their lack of precision; they consequently achieved the required accuracy by using, in combination, quartz crystals and hybrid passive components, known as delay lines. All silicon delay lines offer single chip reliability, economy and significantly greater precision due to their laser-defined specifications. Direct laser writing provides precise accuracy and, because the products are defined in the final stage of manufacturing, a broad product mix is available without losing the economic benefits of standard intergrated circuit production. Customers are provided maximum flexibility, as well as the option of purchasing tailor-made products at the approximate cost of standard, off-the-shelf solutions. These all silicon products can be retrofitted into existing systems which otherwise utilize hybrid approaches as well as designed into new systems.

DS1000 5 TAP Delay Line
DS1010 10 TAP Delay Line
DS1013 3 in 1 Delay Line
DS1007 7 in 1 Delay Line
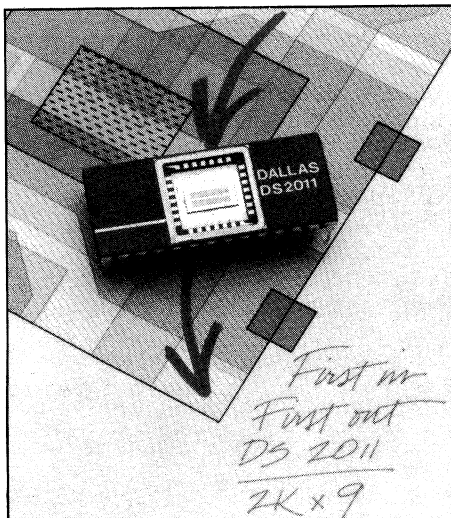
MULTIPORT MEMORY

The existence of many different data transmission rates and standards has created a problem in transporting data among different systems. A receiving system may be too slow to keep up with data sent from another system. First In, First Out (FIFO) memories are capable of providing the necessary elasticity between different data rates.

DS2009 512 × 9 FIFO
DS2010 1K × 9 FIFO
DS2011 2K × 9 FIFO
DS2012 4K × 9 FIFO
DS2013 8K × 9 FIFO
DS9050 PC InterLink
DS2015 4 × 64 Quadport Serial RAM
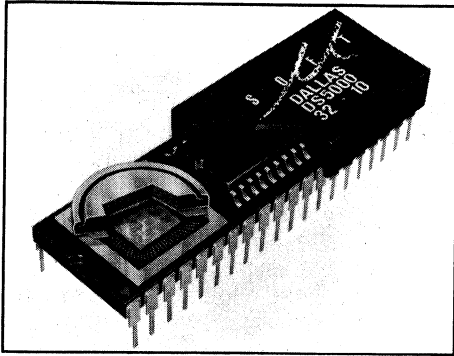
MICROCONTROLLER

The DS5000 Soft Microcontroller stays up-to-date because it was designed for change. Unlike rigid ROM or EPROM based microcontrollers, all of the Soft Microcontroller memory is high performance, read/write, and nonvolatile for more than ten years. The DS5000 is equipped with up to 64K bytes of nonvolatile SRAM which can be dynamically partitioned to fit program and data storage requirements of a particular task. As a result of sophisticated crashproofing circuitry, processing of a task can resume after a power outage. A built-in encrypter prevents unauthorized access to resident application software. The pinout and instruction set match the industry standard 8051 microcontroller. The DS5000T Time Microcontroller can log events and schedule activities according to calendar time. Additional information is available in a special publication called the Soft Microcontroller User Guide. The DS5000K evaluation kit includes a sample DS5000, documentation, in-system loader hardware and DOS compatible software for use with a personal computer. For extensive development work the DS5000DK in circuit emulator is recommended.

    DS5000 Soft Microcontroller
    DS5000T Time Microcontroller
    DS5000K Evaluation Kit
    DS5000DK Development Kit
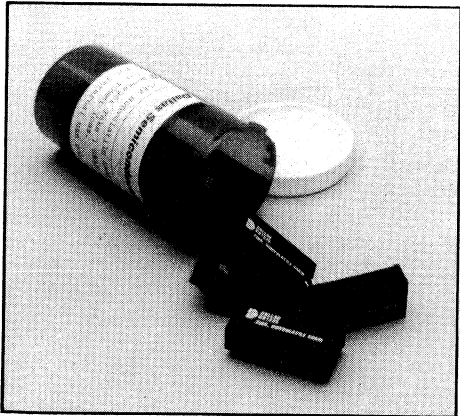
NONVOLATILE SRAM

SRAMS have always had the undesirable characteristics of data loss when power is disrupted. Dallas Semiconductor has combined its knowledge of ultra low power CMOS SRAMs with improvements in long life embedded lithium power sources to develop a family of Nonvolatile SRAMs. Nonvolatile SRAMs integrate a lithium power source and intelligent control circuitry to retain data even in the absence of system power. The control circuit, by monitoring the level of system voltage available to the memory at all times, switches to the lithium power source when necessary, and also protects the memory contents against inadvertent change during system power fluctuations. A lithium power source provides backup power for more than 10 years in the absence of system power. Nonvolatile

SRAMs are packaged to fit into existing sockets and can replace other widely used memory devices. These products perform better in many applications than EEPROMs, EPROMs, or shadow RAMs because they provide unlimited data write cycles, safeguard against corrupted data and write data in as fast as 70 ns.

DS1220 2K × 8 24 pin Nonvolatile SRAM
DS1225 8K × 8 28 pin Nonvolatile SRAM
DS1235 32K × 8 28 pin Nonvolatile SRAM
DS1245 128K × 8 32 pin Nonvolatile SRAM
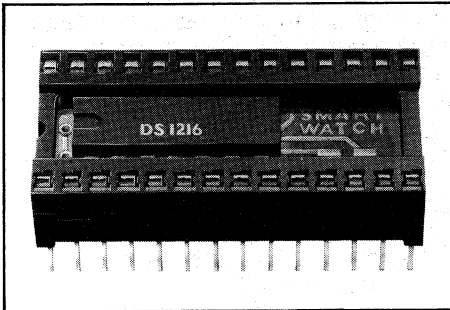
INTELLIGENT SOCKETS

Often, after a design is complete, the manufacturer may desire to enhance functionality because of increased competition from newer products. The equipment manufacturer is forced either to avoid adding features or design a new system. Dallas Semiconductor has incorporated active electronics in connectors which can be plugged into a system and add capabilities without requiring substantive changes in the existing system. For example, many systems manufacturers desire the capability to make RAMs in existing systems nonvolatile. In this instance, they can unplug a memory circuit in a system currently in use, plug the SmartSocket into that space, and plug the memory circuit into the SmartSocket. Another example is a requirement in many existing systems to monitor and record time of day. The SmartWatch plugs into existing systems and keeps time of day to hundredths of a second while also making memory circuits nonvolatile.

DS1213 SmartSocket — makes CMOS RAM nonvolatile
DS1216 SmartWatch — adds the ability to time stamp and date events
DS1264 LCA SmartSocket — maintains logic in the absence of power
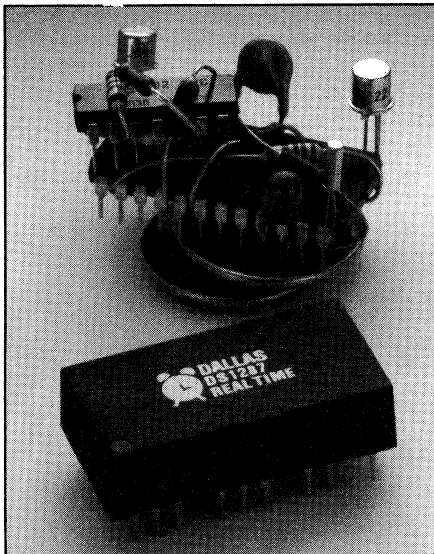
TIMEKEEPING

Systems benefit by knowing the time-of-day, but the use of this feature has been limited by its expense and high component count. A self-contained lithium energy source in conjunction with a silicon chip and quartz form a permanently powered clock/calendar within a single component. The DS1287 RealTime replaces 20 parts used in

the IBM AT and PS/2 compatible computers including an MC146818 Real Time Clock plus RAM.

    DS1202 Serial Timekeeper
    DS1215 Timechip
    DS1287 RealTime
    DS1286 WatchDog

USER INSERTABLE MEMORY

Manufacturers of equipment often wish to facilitate user configuration of their standard products. In many instances, user insertable solid state memories offer distinct advantages over alternative media, such as magnetic tape or disk. Such memories, however, demand specialized packaging capable of withstanding harsher environmental conditions than those normally encountered by semiconductor memory circuits. A family of Nonvolatile SRAMs has been specifically developed to address this application sector. These products range in density from 1024 bits to 32,000,000 bits, the largest of which replaces rotating memory subsystems in certain personal computer systems.

    DS1201 1K bit Electronic Tag
    DS1217A up to 256K bit Nonvolatile Read/Write Cartridge
    DS1217M up to 4M bit Nonvolatile Read/Write Cartridge
    DS6010 P.C. Port
    DS9020 Cartridge Clip

SECURITY PRODUCTS

In an information age, there is an increasing demand to provide security for intellectual property and other data beyond legal measures currently available. Prominent examples are publishers and authors of premium-priced personal computer software who have strong motivation to protect their products from unauthorized use. Software based copy protection systems interfere with the need to make legitimate backup copies or execution from hard disks. The Electronic Key is a postage stamp-sized package that is distributed with each software package sold and must be present whenever users want to use the controlling access to buildings, automobiles and other equipment.

    DS1204 Electronic Key
    DS1207 Time Key
    DS1255 Key Ring
    DS1255C Evaluation Kit for IBM P.C.
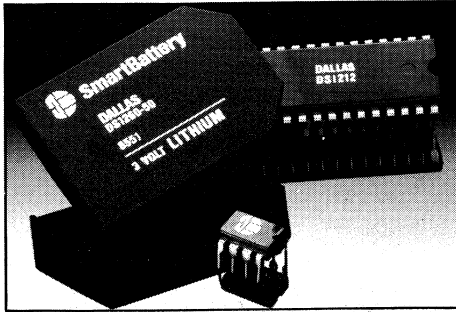
INTEGRATED BATTERY BACKUP

Microprocessor based systems lose information when affected by a loss of power. When system power is resumed, the task that was being performed at the time of power loss must be restarted. Uninterruptible power supplies have historically been provided as relatively expensive, bulky, external units. A solution to this problem is necessitated in industrial automation applications and in systems which are located in remote sites or otherwise difficult to reprogram when information is lost. Integrated Battery Backup consists of a three part chip set which operates in three steps. First, the Power Monitor warns a microprocessor of an impending power failure before it happens, providing time for critical data to be stored in nonvolatile memory before system power is lost. Second, the Nonvolatile Controller/ Decoder converts RAM into nonvolatile memories and safeguards against RAM data loss during power up and down transients, by automatically switching to battery power when system power failure occurs. Third, the SmartBattery supplies uninterruptible power in the absence of system power to maintain data in nonvolatile memory.

> DS1210 Single RAM Controller
> DS1221 Four RAM Controller
> DS1211 Eight RAM Controller
> DS1212 Sixteen RAM Controller
> DS1234 Conditional RAM Controller
> DS1231 Power Monitor
> DS1260 SmartBattery
> DS1259 BatteryManager
> DS1237 NV DRAM Controller
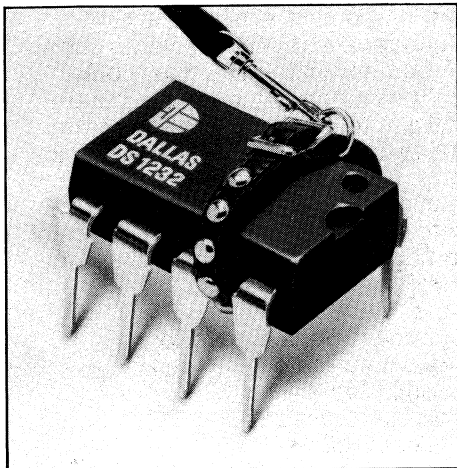
SYSTEM EXTENSION

These CMOS products extend the usefulness of systems without encumbering design. The Micro-Monitor acts as a "watchdog" for system malfunction by checking the three most important indicators of correct microprocessor operation-power supply, software execution and override push-button. If it detects a problem, the Micro-Monitor shuts down the system, then resets it for correct operation. The Eliminator replaces the equivalent of an 8 or 16 station manual DIP switch, thus eliminating burdensome hand setting of mechanical switches. Five volt powered RS232 transceivers are available in both dual and triple versions. The same five volt supply that powers logic generates RS232 voltage levels.

> DS1236 MicroManager
> DS1232 MicroMonitor

DS1290/91 Eliminator, 8-Station
DS1292/93 Eliminator,16-Station
DS1206 Phantom Interface
DS1223 Configurator
DS1222 Bank Switch
DS232/DS1228 R232 Transceiver, Dual
DS1229 RS232 Transceiver, Triple
DS1275 Line Powered
    RS232 Transceiver
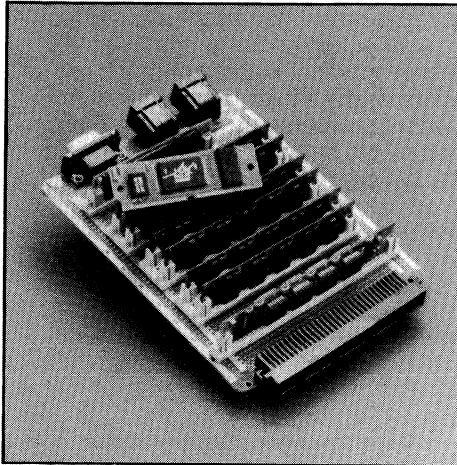
SipStiks™

Systems snap together with SipStik sub-assemblies from Dallas Semiconductor. SipStiks are leadless carriers of components with high silicon content using JEDEC standard configurations. Their low profile form factor permits high density yet offers the advantages of modularity. Their major building blocks are pretested and ready for final assembly into a planar motherboard fitted with AMP MicroEdge connectors as required by a particular application.

    DS2217 SRAM SipStik
    DS2219 DRAM SipStik
    DS2250 Soft Micro SipStik
    DS2250T Time Micro SipStik
    DS2245 Soft Modem SipStik
    DS2249 Data Access Arrangement SipStik
    DS2212 FIFO SipStik
    DS2280 T1 SipStik
    DS2268 ADPCM Compression SipStik
    DS6040 Wireless SipStik
    DS2260 Feedback Control SipStik
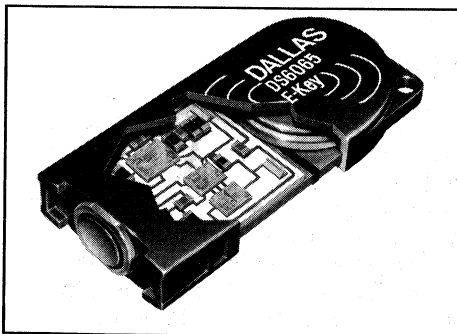
WIRELESS PRODUCTS

Proximity Tags and Proximity Keys can communicate with a personal computer using CMOS Micropower Receiver/2-to 3 Wire Converter chips and a base RF Communicator. The chips contain wake-up circuitry, amplifiers, filters, timing generators, waveform interpreters, formating and control logic necessary to form a bi-directional 5 foot link between portable units and bases. The ultra low power consumption of the chips enable a single 3 volt lithium energy cell to be a permanent source of power for receiving, storing, and transmitting data.

    DS1203 MicroPower Receiver
    DS1209 2-to 3-Wire Converter
    DS1280 Bytewide to Serial Converter
    DS6068 RF Communicator
    DS6065 Proximity Key
    DS6066 Proximity Tag
    DS6040 Wireless SipStik
    DS6068K Wireless Starter Kit
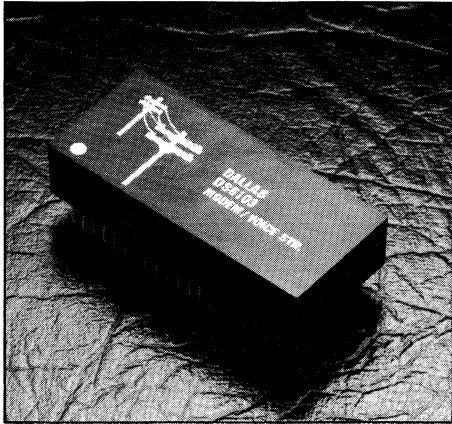
MODEM

These miniature components comply with FCC part 68 registration. The DS6101 Modem is bell 212A compatible (1200/300 bps) with DTMF generation/detection, audio mode operation, and advanced line monitoring functions. The DS6103 Modem provides voice synthesis. The DS6112 and DS2249 Data Access Arrangements (DAA) are also available as a stand alone interface to the public switch telephone network.

DS6101 1200 bps Modem
DS6103 1200 bps Modem with Voice
DS2245 1200 bps Soft Modem
DS6112 DAA
DS2249 DAA SipStik
DS6070 Tele Micro
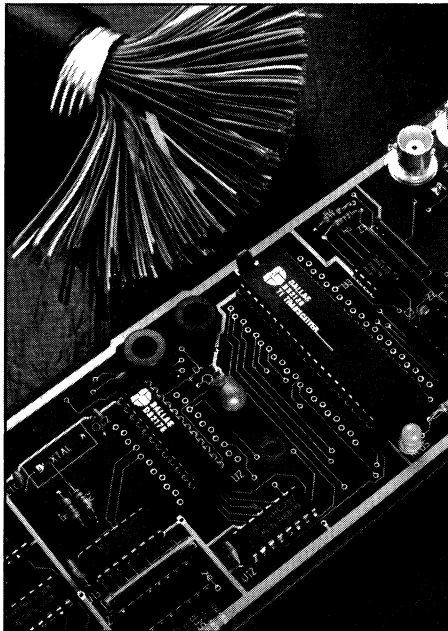
TELECOMMUNICATONS

An emerging and rapidly growing market exists for high capacity voice, data and video transmission. High capacity digital links in North America and Europe are known as T-1 and CEPT, respectively. Circuits designed for these protocols can substantially shorten the time required for OEMs to develop products that access these networks and can reduce system sizes. A comprehensive chip set developed by Dallas Semiconductor addresses the requirements of these protocols and includes an integrated circuit that doubles the capacity of existing voice communication links through digital signal processing compression techniques. Complete product specifications available in a supplemental telecommunications data book.

DS2180A Transceiver, T1
DS2181 Transceiver, CEPT
DS2175 Transmit/Receive Elastic Store
DS2176 Receive Elastic Store
DS2186 Transmit Line Interface
DS2187 Receive Line Interface
DS2190 Network Interface Unit
DS2167 ADPCM Processor
DS2280 T1 SipStik
DS2268 ADPCM Compression SipStik

Product Data Sheets

Dallas Semiconductor
ADPCM ARRAY

FEATURES

- High-density, multi-channel speech compression system provides 12 or 24 full duplex channels on a 3 x 3 inch board.

- Based on high-performance DS2167/68 ADPCM processors. DS2157 uses the DS2167 and supports the July 1986 T1Y1 recommended algorithm. DS2158 supports the "old" CCITT G.721 algorithm.

- Flexible data bussing scheme to accomodate user's backplane data format and rate.

- Microcontroller-compatible port for system configuration. On-board power monitor provides system reset.

- Arrays are easily cascaded for even higher system density.
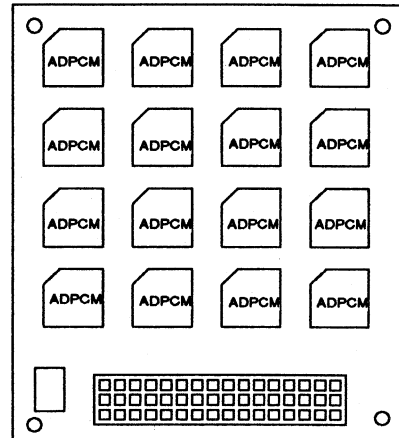
DESCRIPTION

The DS2157 and DS2158 ADPCM Arrays use surface-mount technology and the DS2167/68 ADPCM processors to yield 12 or 24 full-duplex channels in nine square inches. The DS2157 array features the DS2167Q processor which implements the July 1986 T1Y1 recommended ADPCM algorithm. The DS2158 array features the DS2168Q processor which implements the "old" CCITT G.721 algorithm. A suffix of "-1" indicates a 12-channel array; a "-2" indicates a a 24-channel array. The PCM data interfaces are organized into four independent busses which may be configured to best suit the data format on the user's system backplane. The array also includes input signal buffering and a power-monitor reset circuit.

SYSTEM PIN-OUT Figure 1
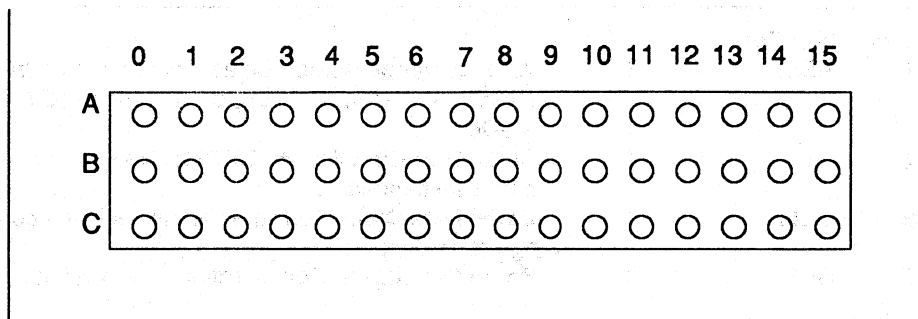
PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
Low X-Side Data Interface			
A3	CLKX LO	I	Data Clock
B5	FSX LO	I	Frame Sync
A4	XIN LO	I	Data Input
B3	XOUT LO	O	Data Output
Low Y-Side Data Interface			
C4	CLKY LO	I	Data Clock
B6	FSY LO	I	Frame Sync
C7	YIN LO	I	Data Input
C6	YOUT LO	O	Data Output
High X-Side Data Interface			
C11	CLKX HI	I	Data Clock
B12	FSX HI	I	Frame Sync
C9	XIN HI	I	Data Input
C8	XOUT HI	O	Data Output
High Y-Side Data Interface			
B13	CLKY HI	I	Data Clock
B10	FSY HI	I	Frame Sync
B11	YIN HI	I	Data Input
B9	YOUT HI	O	Data Output

PIN DESCRIPTION Table 2

PIN	SYMBOL	TYPE	DESCRIPTION
Serial Configuration Port			
B7	ASEL	I	**Array Address Select.** Selects processor addresses 0 through 23 (ASEL = VSS) or 32 through 55 (ASEL = VDD)
B4	$\overline{CS}$	I	**Serial Port Chip Select.** Drive low to initiate a serial port write sequence.
C3	SCLK	I	**Serial Data Clock.** Rising edge clocks in the configuration data.
C5	SDI	I	**Serial Data Input.** Configuration data, written LSB first.
System Control			
B1	MCLK	I	**Master Clock.** 10 MHz clock for ADPCM processing engine. May be asynchronous with other clocks.
C10	$\overline{RST}$	O	**Reset Output.** Normally high signal which transitions low at power on or when RSTIN is activated.
C12	$\overline{RSTIN}$	I	**Reset Input.** A high-low-high transition initializes the array and sets all processors idle. Input is internally pulled high with a nominal 10K ohm resister, and may be left unconnected if not used.
Power			
A5-A9, B8			
	VDD		**Positive Supply.** 5.0 volts.
A0-2, A10-15, B0, B2, B14-15, C0-2, C13-15			
	VSS		**Signal Ground.** 0.0 Volts.

BLOCK DIAGRAM Figure 2
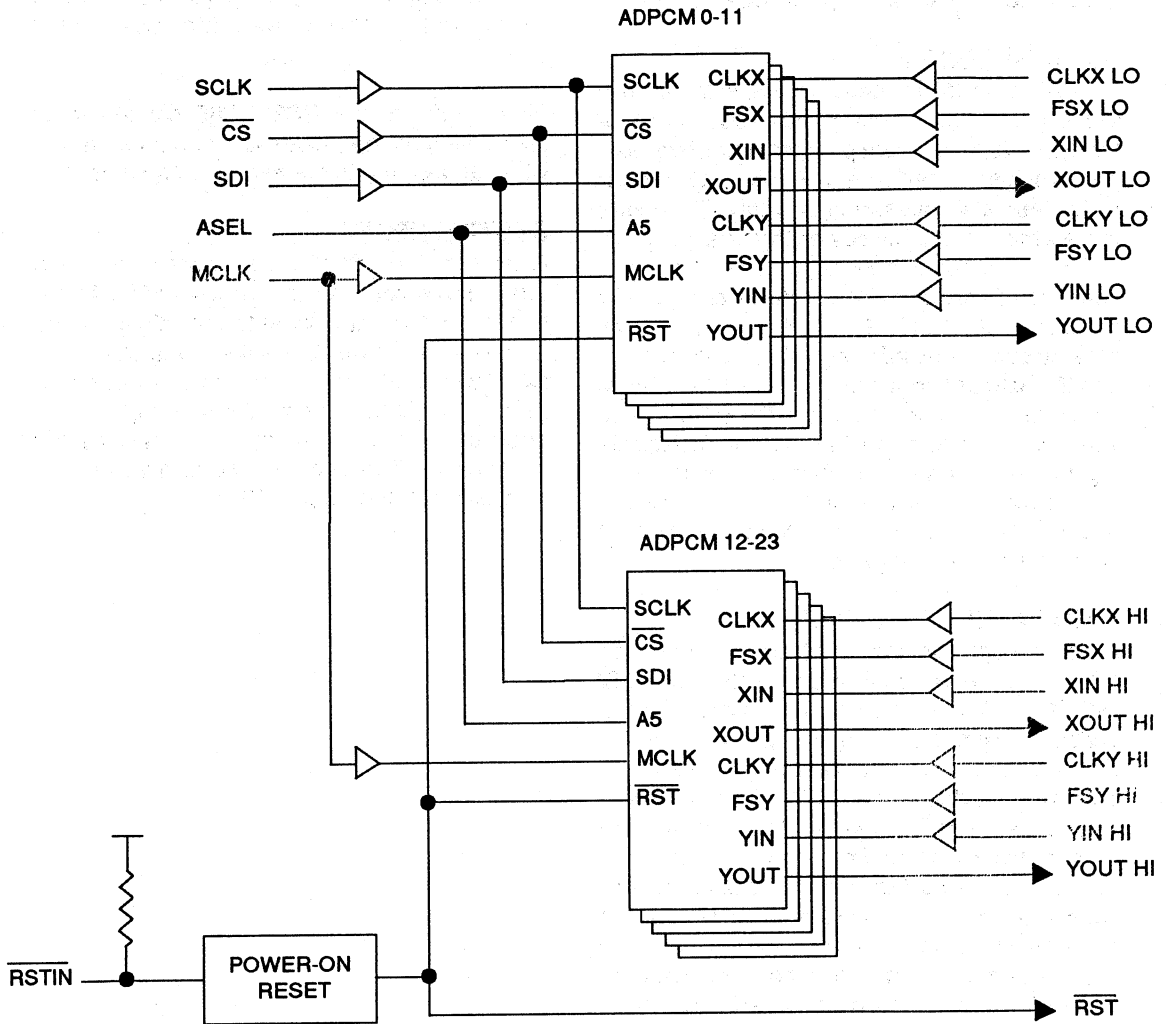
MASTER CLOCK

The MCLK master clock input drives the ADPCM processors. This clock is 10 MHz and should be generated by a stable, crystal-based oscillator.

DATA BUSSING

The 24 ADPCM Processors are split into two groups of 12, and each group is bussed separately. In addition, each processor has two independent data interfaces (X-side and Y-side) which are also bussed separately. Therefore, there are four data busses on the array; the low-X, low-Y, high-X and high-Y busses. Each bus consists of four signals: a data clock (typically running at 1.544 MHz, 2.048 MHz or 4.096 MHz), a frame synchronization signal (typically 8 KHz), a PCM/ADPCM data input, and a PCM/ADPCM data output. Please refer to the DS2167/68 data sheet for information on the PCM interface clocking and data signals. The busses may be operated separately, processing 12 channels per bus, or tied together to increase the number of channels processed per bus.

SYSTEM CONFIGURATION

All processors on the array share a common three-wire serial control port interface (CS/ ,SCLK, and SDI). This interface is directly compatible with popular microcontrollers such as the DS5000 and 8051. The port is used to define operating modes and timeslots for the processors in the array. Data written to the control port is either two bytes (address/command and control) or four bytes (address/command, control, input timeslot and output timeslot) in length. The address/command byte contains a field which specifies processor address (between 0 and 63) and a bit which selects a data interface (either X or Y). If the address in this byte matches the address assigned to a processor in the array, then that processor will accept the following configuration data.

The ASEL input selects the addressing to the processors. With ASEL tied to VSS, the twelve processors on the low-X and low-Y busses are addressed as 0 through 11, and the 12 processors on the high-X and high-Y busses are addressed as 12 through 23. With ASEL tied to VDD, the processors on the low-X and low-Y busses are addressed as 32 through 43, and the processors on the high-X and high-Y busses are addressed as 44 through 55. This feature allows two arrays to share the same three-wire control port.

Please refer to the DS2167/68 datasheet for information on the processor configuration registers and writing to the serial control port.

SYSTEM RESET

A system reset initializes all processors in the array and places them into an idle mode. An on-board power monitor will automatically generate a reset when power is applied. In addition, the RSTIN/ input allows the array to be reset externally. This input is internally tied high with a nominally 10K ohm resistor and may be left unconnected if not used. The system reset signal is available at the output RST/.

48-CHANNEL SYSTEM EXAMPLE Figure 3
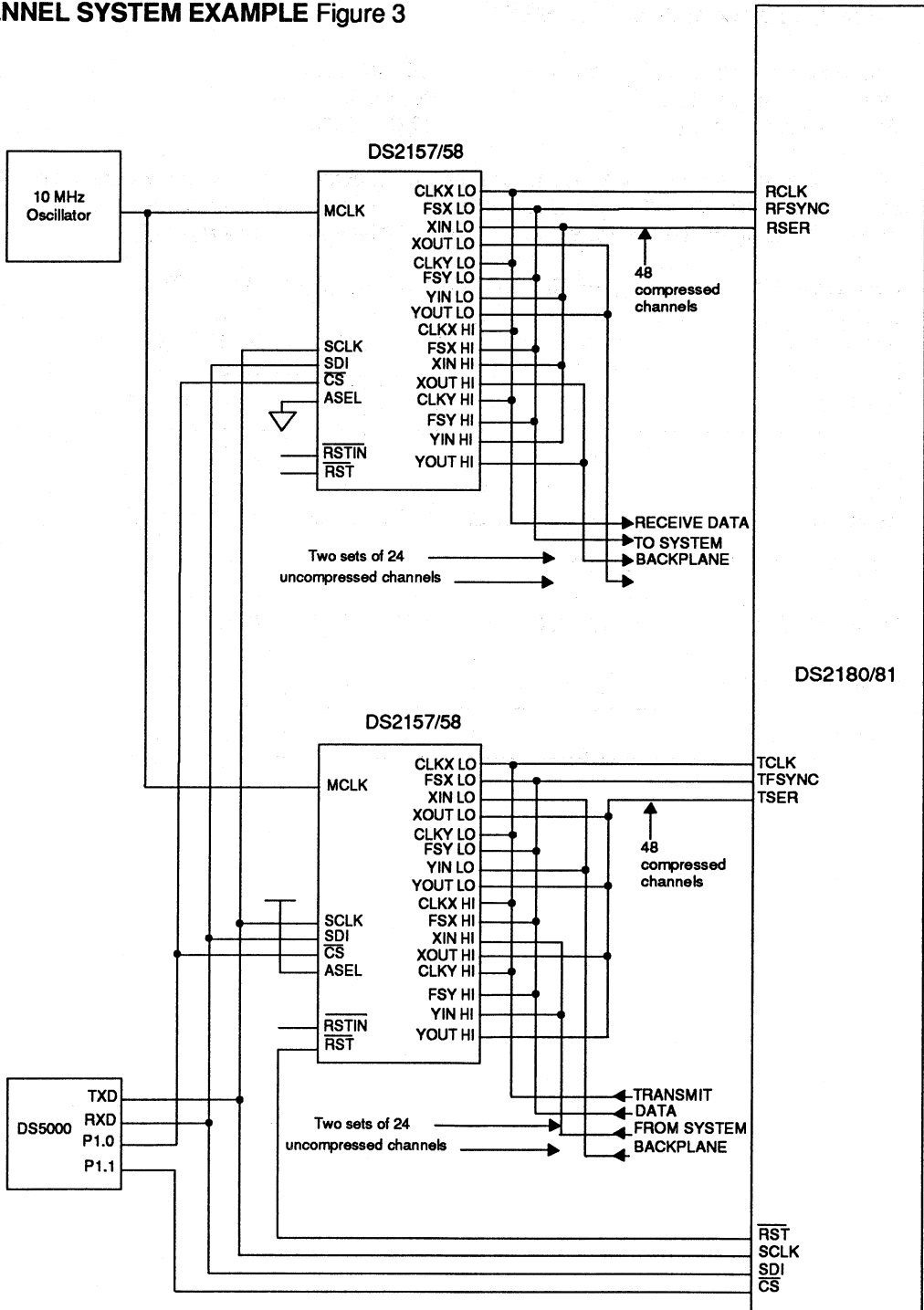
ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground   -1.0V to +7.0V
Operating Temperature   0°C to 70°C
Storage Temperature   -40°C to 70°C

*This is a stress rating only and functional operation of the system at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{DD}+0.3$	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	4.55		5.5	V	

CAPACITANCE (TA = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			20	pF	
Output Capacitance	C_{OUT}			120	pF	

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Current	I_{DD}			985	ma	1,2
Standby Current	I_{DDPD}			75	ma	1,2,3
Input Leakage	I_{IL}					
MCLK		-200		+40	u a	
RSTIN/		-725		+50	u a	
all other inputs		-100		+20	u a	
Output Current @ 2.4V	I_{OH}					
RST/		-0.7			ma	
all other outputs		-1.0			ma	
Output Current @ 0.4V	I_{OL}	4.0			ma	
I/O Leakage	I_{IO}	-12.0		+12.0	u a	

NOTES:
1. CLKX LO = CLKY LO = CLKX HI = CLKY HI = 1.544 MHz, MCLK = 10 MHz
2. Outputs open, inputs swinging full supply levels.
3. All channels of all processors programmed to "idle power down" mode.

2

PCM INTERFACE
A.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
MCLK	tPM		100		ns	
MCLK Pulse Width	tWMH,tWML		50		ns	
MCLK Rise and Fall Times	tRM,tFM		5	10	ns	
CLKX, CLKY Period	tPXY		488		ns	4
CLKX, CLKY Pulse Width	tWXYH, tWXYL		244		ns	
CLKX, CLKY Rise and Fall Times	tRXY, tFXY		10	20	ns	
Hold Time from CLKX, CLKY to FSX, FSY	tHOLD	0			ns	1
Set Up Time from FSX ,FSY to CLKX, CLKY low	tSF	50			ns	1
Hold Time from CLKX, CLKY low to FSX, FSY low	tHF	100			ns	1
XIN, YIN Set Up to CLKX, CLKY LowtSD		50			ns	1
XIN, YIN Hold CLKX, CLKY Low	tHD	50			ns	1
Delay Time from CLKX, CLKY to Valid XOUT, YOUT	tDXYO	5		150	ns	2
Delay Time from CLKX, CLKY to XOUT, YOUT Tristated	tDXYZ	20		150	ns	1,2,3

NOTES:
1. Measured at VIH = 2.0 OR VIL = 0.8V and 10 ns maximum rise and fall times.
2. Load = 150 pF + 2 LSTTL loads.
3. For LSB of PCM byte or ADPCM nibble.
4. Maximum width of FSX, FSY is one CLKX, CLKY period.

PCM INTERFACE A.C. TIMING DIAGRAM Figure 4
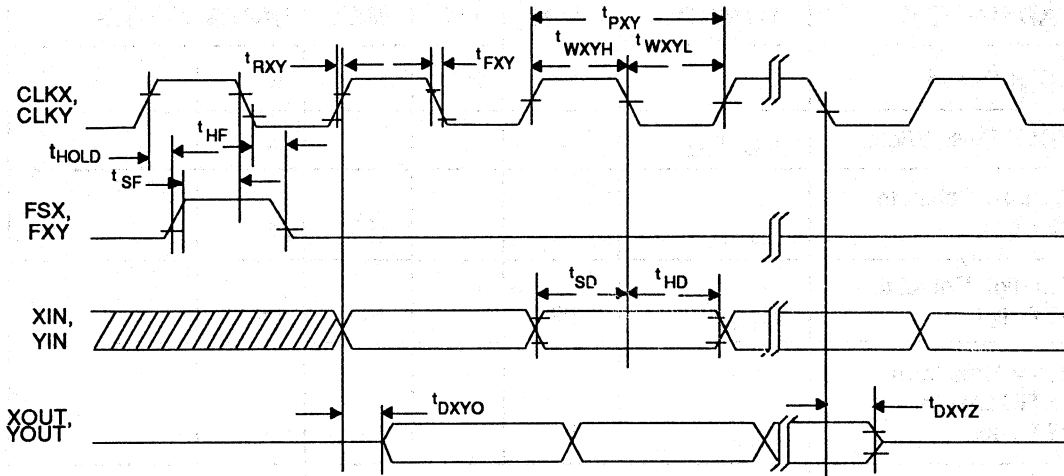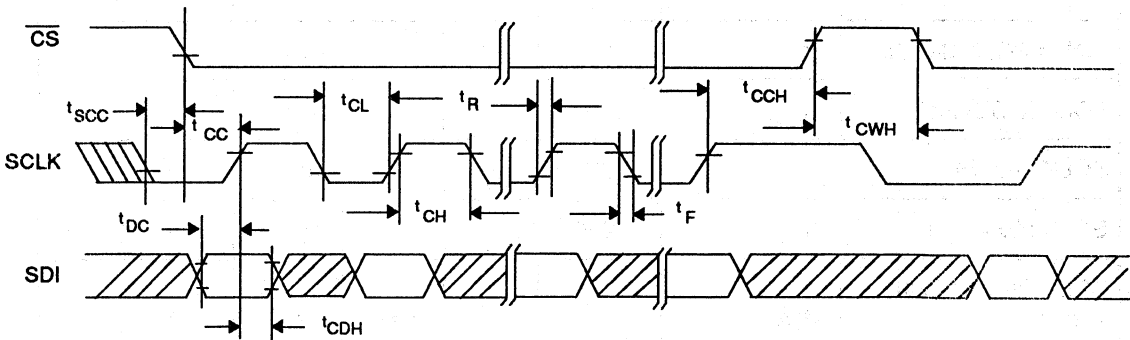
SERIAL PORT WRITE A.C. TIMING DIAGRAM Figure 5

MASTER CLOCK/RESET
A.C. ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
MCLK Period	t_{PM}		100		ns	
MCLK Pulse Width	t_{WMH}, t_{WML}	50			ns	
V_{DD} Low Detect to RST Low	t_{RSTPD}			100	ns	
V_{DD} High Detect to RST High	t_{RSTX}	250		1000	ms	
Delay Time from RSTIN Low to RST Low	t_{RSTIN}	20			ms	
Delay Time from RSTIN High to RST High	t_{RSTX}	250		1000	ms	
RSTIN Pulse Width	t_{WRL}		1		ms	

SERIAL PORT
A.C. ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SDI to SCLK Set Up	t_{DC}	55			ns	1
SCLK to SDI Hold	t_{CDH}	55			ns	1
SCLK Low Time	t_{CL}	250			ns	1
SCLK High Time	t_{CH}	250			ns	1
SCLK Rise and Fall Times	t_R, t_F			100	ns	1
CS to SCLK Set Up	t_{CC}	50			ns	1
SCLK to CS Hold	t_{CCH}	250			ns	1
CS Inactive Time	t_{CWH}	250			ns	1
SCLK Set Up to CS Falling	t_{SCC}	50			ns	1

NOTE: 1. Measured at V_{IH} = 2.0 or V_{IL} = 0.8V and 10 ns maximum rise and fall times.

MASTER CLOCK/RESET A.C. TIMING Figure 6

Dallas Semiconductor
ADPCM Processor

<div align="right">

DS2167
DS2168

</div>
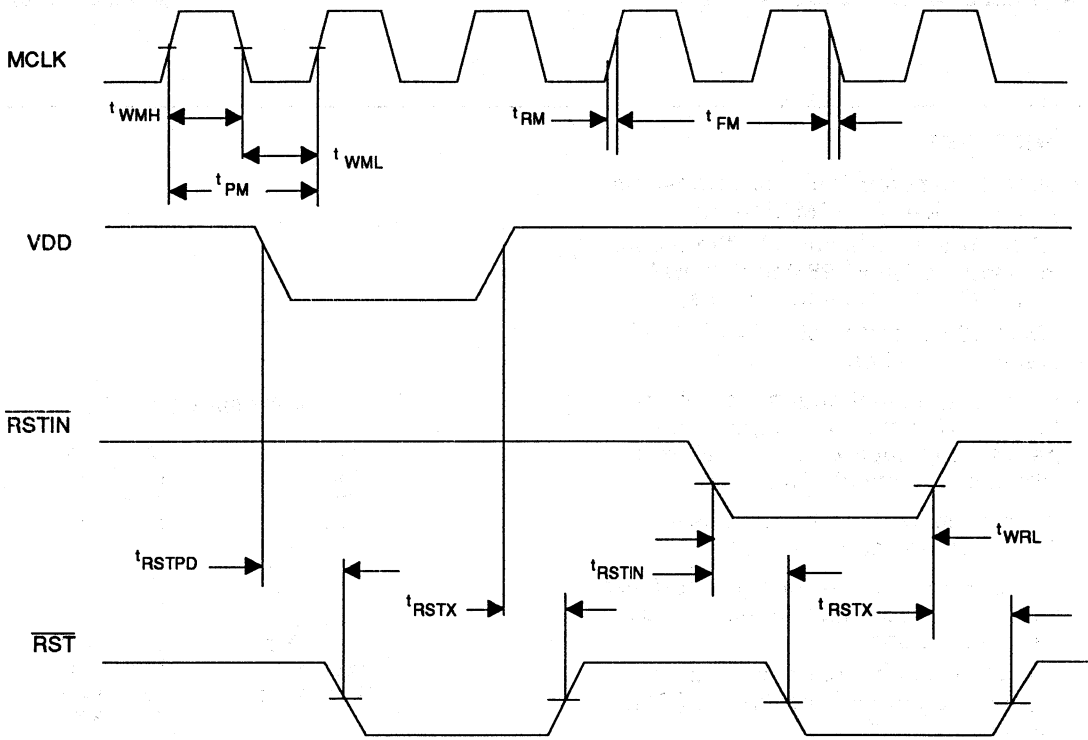
FEATURES

- Speech compression chip compatible with standard ADPCM algorithms:

  - DS2167 supports "new" T1Y1 recommendations (July 1986) and "new" CCITT G.721 recommendations

  - DS2168 supports "old" CCITT G.721 recommendations

- Dual independent channel architecture—device may be programmed to perform full duplex, 2-channel expansions, or 2-channel compressions

- Interconnects directly with u-law or A-law combo-codec devices

- Serial PCM and control port interfaces minimize "glue logic" in multiple channel applications

  - On-chip channel counters identify input and output timeslots in TDM-based systems

  - Unique addressing scheme simplifies device control; 3-wire port shared among 64 devices

  - Bypass and idle features allow dynamic allocation of channel bandwidth, minimize system power requirements

- Hardware mode intended for stand-alone use

  - No host processor required

  - Ideal for voice mail applications

- 28-pin surface-mount package available, designated DS2167Q/DS2168Q

PIN CONNECTIONS

$\overline{RST}$	1	24	VDD
TM0	2	23	YIN
TM1	3	22	CLKY
A0	4	21	FSY
A1	5	20	YOUT
A2	6	19	$\overline{CS}$
A3	7	18	SDI
A4	8	17	SCLK
A5	9	16	XOUT
SPS	10	15	FSX
MCLK	11	14	CLKX
VSS	12	13	XIN
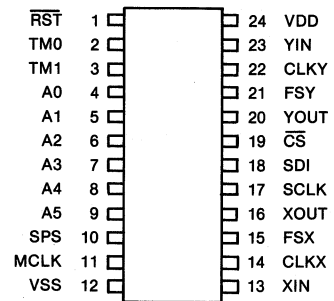
DESCRIPTION

The DS2167 and DS2168 are dedicated digital signal processor (DSP) CMOS chips optimized for Adaptive Differential Pulse Code Modulation (ADPCM) based speech compression algorithms. The devices halve the transmission bandwidth of "toll quality" voice from 64K to 32K bits/second and are utilized in PCM-based telephony networks.

PRODUCT OVERVIEW

The DS2167 and DS2168 contain three major functional blocks: a high performance (10 MIPS) DSP "engine," two independent PCM data interfaces ("X" and "Y") which connect directly to serial time division multiplexed (TDM) backplanes and a microcontroller-compatible serial port for "on-the-fly" device configuration. A 10 MHz master clock is required by the DSP engine. The devices' dual channel architecture supports full duplex, dual compression or dual expansion operation. The PCM data interfaces support 1.544, 2.048 and 4.096 MHz data rates. Each device samples the serial PCM or ADPCM bit stream during a user-programmed input timeslot, processes the data, and outputs the result during a user-programmed output timeslot.

Each PCM interface has a control register which specifies functional characteristics (compress, expand, bypass and idle), data format (u-law or A-law) and algorithm reset control. With the SPS pin strapped high, the software mode is enabled and the serial port is used to program control and timeslot registers. In this mode, a novel addressing scheme allows multiple devices to share a common three-wire control bus, simplifying system level interconnect.

With SPS low the hardware mode is enabled. This mode disables the serial port and maps appropriate control register bits to address and port inputs. Under hardware mode, no host controller is required and all PCM I/O defaults to timeslot 0. This stand-alone mode is compatible with popular codecs.

DS2168 BLOCK DIAGRAM Figure 1

2

PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	$\overline{\text{RST}}$	I	**Reset.** A high-low-high transition clears all internal registers and resets both algorithms. The device should be reset on system power-up, and/or when changing to/from hardware mode.
2 3	TM0 TM1	I	**Test Modes 0 and 1.** Tie to VSS for normal operation.
4 5 6 7 8 9	A0 A1 A2 A3 A4 A5	I	**Address Select.** A0 = LSB; A5 = MSB. Must match address/ command word to enable serial port write.
10	SPS	I	**Serial Port Select.** Tie to VDD to select the serial port, to VSS to select the hardware mode.
11	MCLK	I	**Master Clock.** 10 MHz clock for ADPCM processing "engine;" may asynchronous to SCLK, CLKX AND CLKY.
12	VSS	—	**SIGNAL GROUND.** 0.0 volts.
13	XIN	I	**X Data In.** Sampled on falling edge of CLKX during selected timeslots.
14	CLKX	I	**X Data Clock.** Data clock for X side PCM interface, must be coherent and rising edge aligned with FSX.
15	FSX	I	**X Frame Sync.** 8 KHz frame sync for X side PCM interface.
16	XOUT	O	**X Data Out.** Updated on rising edge of CLKX during selected timeslots.
17	SCLK	I	**Serial Data Clock.** Used to write serial port registers.
18	SDI	I	**Serial Data In.** Data for on-board control registers. Sampled on rising edge of SCLK.
19	$\overline{\text{CS}}$	I	**Chip Select.** Must be low to write the serial port.
20	YOUT	O	**Y Data Out.** Updated on rising edge of CLKY during selected timeslots.
21	FSY	I	**Y Frame Sync.** 8 KHz frame sync for Y side PCM interface.
22	CLKY	I	**Y Data Clock.** Data clock for Y side PCM interface; must be coherent and rising edge aligned with FSY.
23	YIN	I	**Y Data In.** Sampled on falling edge of CLKY during selected timeslots.
24	VDD	—	**Positive Supply.** 5.0 volts.

HARDWARE RESET
$\overline{\text{RST}}$ allows the user to reset both channel algorithms and internal register contents. This input must be held low for at least 1 millisecond on system power-up after master clock is stable to assure proper initialization of the device. $\overline{\text{RST}}$ should also be asserted when changing to/from the hardware mode. $\overline{\text{RST}}$ clears all bits of the control register except IPD; IPD is set for both channels, powering down the device.

HARDWARE MODE
The hardware mode is intended for preliminary system prototyping or for applications which do not require the features of the serial port. Tying $\overline{\text{SPS}}$ to VSS disables the serial port, clears all internal registers and maps IPD, $u/\overline{A}$ and CP/$\overline{\text{EX}}$ of the X and Y side interfaces to the port and address inputs. Input and output timeslots for the X and Y side interfaces are fixed at 0. Such applications include, but are not limited to: 1) systems in which timeslot and algorithm are fixed, 2) stand-alone ADPCM combo applications, 3) "hardware" oriented systems where no host controller is available.

2

HARDWARE MODE Table 2

PIN #/NAME	REG. LOCATION	NAME AND DESCRIPTION
4/A0	CP/$\overline{\text{EX}}$ (X)	**Channel X coding** 0 = Expand 1 = Compress
6/A2	$u/\overline{A}$ (X)	**Channel X data format** 0 = A-law 1 = u-law
7/A3	CP/$\overline{\text{EX}}$ (Y)	**Channel Y coding** 0 = Expand 1 = Compress
9/A5	$u/\overline{A}$ (Y).2	**Channel Y data format** 0 = A-law 1 = u-law
18/SDI	IPD (Y)	**Y idle select** 0 = Channel active 1 = Channel idle
19/$\overline{\text{CS}}$	IPD (X)	**X idle select** 0 = Channel active 1 = Channel idle

NOTES:
1. SCLK, A1 and A4 must be tied to VSS when the hardware mode is selected.

2. When both X and Y sides are idled; the devices enter a stand-by mode which significantly reduces power consumption.

3. The DS2167 will power-up within 200 milliseconds after the X or Y side is reactivated (SDI and/or $\overline{\text{CS}}$ not equal to 0) from standby.

4. The DS2168 must be hardware reset when reactivated from stand-by. Power-up occurs immediately after the reset.

COMBO CODEC HARDWARE MODE INTERCONNECT Figure 2

POWER ON RESET
(DS1231)

TRANSMIT FRAME SYNC
TRANSMIT DATA CLOCK

VCC	MCLKX	RST	VDD	
VBB	DX	SCLK	A0	
GNDA	FSX	XIN	A5	TP3054 (u-LAW)
TSX	BCLKX	FSX	A2	TP3057 (A-LAW)
VFXI+	DR	CLKX	XOUT	TRANSMIT DATA
VFSI−	FSR	YOUT	YIN	RECEIVE DATA
GSX	BCLKR/CLKSEL	FSY	A3	
VFRO	MCLKR/PDN	CLKY	A4	
		SPS	A1	POWER DOWN
		TM0	SDI	ACTIVE
		TM1	CS	
		VSS	MCLK	10 MHZ CLOCK

−5.0 V

TP3054/3057

DS2167/DS2168

TRANSMIT ANALOG INTERFACE

RECEIVE ANALOG INTERFACE

RECEIVE DATA CLOCK

RECEIVE FRAME SYNC

NOTE:
1. TP3054/3057 are National Semiconductor combo-codecs.

40

SOFTWARE MODE

Tying SPS high enables the software mode. In this mode a host microcontroller writes configuration data to the DS2167/68 serial port via inputs SCLK, SDI and $\overline{CS}$. Independent control and timeslot registers establish operating characteristics for the X-side and Y-side PCM interfaces.

ADDRESS/COMMAND BYTE

In the software mode the address/command byte is the first byte written to the serial port; it identifies which of 64 possible ADPCM processors sharing the port wiring is to be updated. Address data must match that at inputs A0-A5. If no match occurs, the device ignores the following configuration data. If an address match occurs, the next three bytes written are accepted as control, input and output timeslot data. Bit ACB.6 determines which side (X or Y) of the device is to be updated.

CONTROL REGISTER

The control register establishes idle, algorithm reset, bypass, data format and channel coding for the selected PCM interface.

The X and Y side PCM interfaces may be independent disabled (output tri-stated) via IPD; when IPD is set for both X and Y interfaces, the device enters a low power stand-by mode. The DS2167 will power-up within 200 milliseconds after the X or Y side is reactivated (IPD = 0) from standby. The DS2168 requires an external hardware reset after IPD is cleared to "wake-up" from standby. The DS2168 will power-up immediately after the low-high transition on $\overline{RST}$.

ALRST resets the algorithm coefficients for the selected channel to their initial values. ALRST will be cleared by the device when the algorithm reset is complete.

The bypass feature is enabled when BYP is set and IPD is clear. During bypass, no expansion or compression of data occurs. This feature allows the user to interchange timeslots under control of the timeslot registers. Bypass operates on "byte-wide" slots when CP/$\overline{EX}$ = 1; on "nibble-wide" slots when CP/$\overline{EX}$ = 0.

A-law ($u/\overline{A}$ = 0) or u-law PCM ($u/\overline{A}$ = 1) coding is independently selected for the X and Y side interfaces by bit u/A. If BYP and IPD are clear, CP/$\overline{EX}$ determines if input data is to be compressed or expanded.

TIMESLOT ASSIGNMENT

On-chip counters establish when PCM data I/O occurs and are programmed via the timeslot registers. Timeslot size (4 or 8 bits wide) is determined by the state of CP/$\overline{EX}$. Timeslots are counted from the rising edge of FSX and FSY.

ADDRESS/COMMAND BYTE Figure 3

(MSB)							(LSB)
—	X/$\overline{Y}$	A5	A4	A3	A2	A1	A0

SYMBOL	POSITION	NAME AND DESCRIPTION
—	ACB.7	Reserved, must be 0 for proper operation.
X/$\overline{Y}$	ACB.6	**X/$\overline{Y}$ Channel Select.** 0 = Update channel Y characteristics 1 = Update channel X characteristics
A5	ACB.5	**MSB of Device Address.**
A4	ACB.4	
A3	ACB.3	
A2	ACB.2	
A1	ACB.1	
A0	ACB.0	**LSB of Device Address.**

CONTROL REGISTER Figure 4

(MSB)							(LSB)
—	—	IPD	ALRST	BYP	u/$\overline{A}$	—	CP/$\overline{EX}$

SYMBOL	POSITION	NAME AND DESCRIPTION
—	CR.7	Reserved, must be 0 for proper operation.
—	CR.6	Reserved, must be 0 for proper operation.
IPD	CR.5	**Idle and Power Down.** 0 = channel enabled 1 = channel disabled (output tri-stated)
ALRST	CR.4	**Algorithm Reset.** 0 = Normal operation 1 = Reset algorithm for selected channel
BYP	CR.3	**Bypass.** 0 = Normal operation 1 = Bypass selected channel
u/$\overline{A}$	CR.2	**Data Format.** 0 = A-law 1 = u-law
—	CR.1	Reserved, must be 0 for proper operation.
CP/$\overline{EX}$	CR.0	**Channel Coding.** 0 = Expand (decode) selected channel 1 = Compress (encode) selected channel

INPUT TIMESLOT REGISTER Figure 5

(MSB)   (LSB)

—	—	D5	D4	D3	D2	D1	D0

SYMBOL	POSITION	NAME AND DESCRIPTION
—	ITR.7	Reserved, must be 0 for proper operation.
—	ITR.6	Reserved, must be 0 for proper operation.
D5	ITR.5	MSB of input timeslot word.
D4	ITR.4	
D3	ITR.3	
D2	ITR.2	
D1	ITR.1	
D0	ITR.0	LSB of input timeslot word.

OUTPUT TIMESLOT REGISTER Figure 6

(MSB)   (LSB)

—	—	D5	D4	D3	D2	D1	D0

SYMBOL	POSITION	NAME AND DESCRIPTION
—	OTR.7	Reserved, must be 0 for proper operation.
—	OTR.6	Reserved, must be 0 for proper operation.
D5	OTR.5	MSB of output timeslot word.
D4	OTR.4	
D3	OTR.3	
D2	OTR.2	
D1	OTR.1	
D0	OTR.0	LSB of output timeslot word.

2

PCM I/O TIMING (1.544 MHZ BACKPLANE) Figure 7
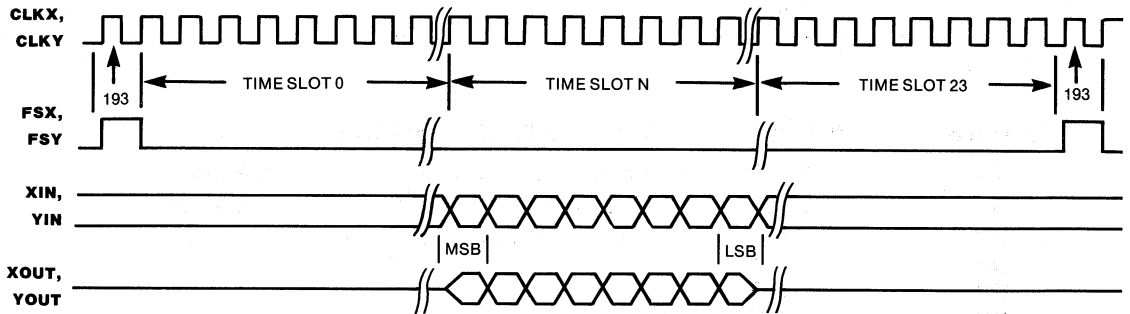
ADPCM I/O TIMING (1.544 MHZ BACKPLANE) Figure 8
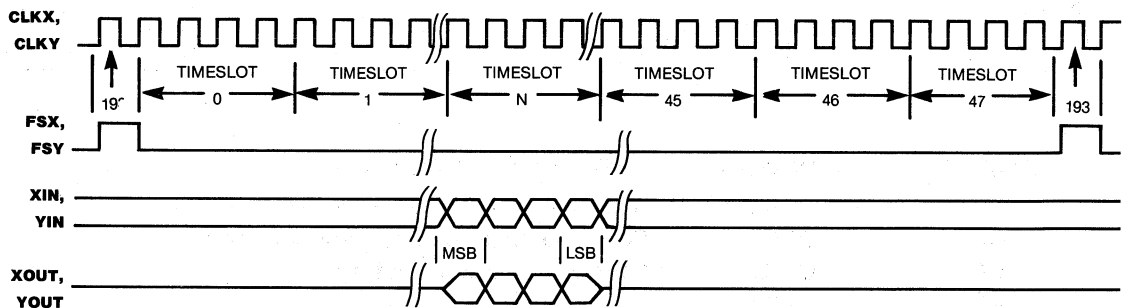
SERIAL PORT WRITE

All port writes are initiated by driving $\overline{CS}$ low and terminated when $\overline{CS}$ returns high. *Data is sampled on the rising edge of SCLK and must be written to the device LSB first.* Writes to the device may be 2 bytes (address/command and control) or 4 bytes (address/command, control, input timeslot and output timeslot) in length. Writes should be terminated on byte boundaries to insure data integrity.

SERIAL PORT WRITE Figure 9

SDI¹ : A0 | A1 | A2 | A3 | A4 | A5 | X/Ȳ | — | CR0 | CR1 | CR2 | CR3 | CR4 | CR5 | CR6 | CR7

ADDRESS/COMMAND — CONTROL
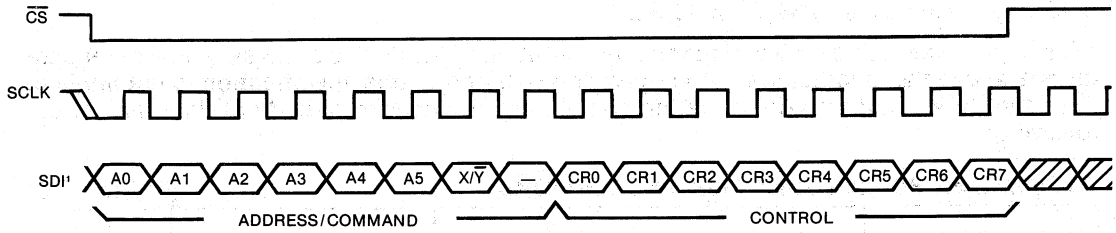
NOTES:
1. 2 byte write shown.

8051-BASED CONTROL SYSTEM Figure 10

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground   -1.0V to +7.0V
Operating Temperature   0°C to 70°C
Storage Temperature   -55°C to +125°C
Soldering Temperature   260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS   (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{CC} + 0.3$	V	
Logic 0	V_{IL}	−0.3		+0.8	V	
Supply	V_{DD}	4.5		5.5	V	

CAPACITANCE   ($t_A = 25$°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	10	pF	

D.C. ELECTRICAL CHARACTERISTICS   (0°C to 70°C $V_{DD} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current (Active)	I_{DDA}		30		mA	1,2
Supply Current (Idle)	I_{DDPD}		1		mA	1,2,3
Input Leakage	I_{IL}	−1.0		+1.0	uA	
Output Leakage	I_{TRI}	−1.0		+1.0	uA	4
Output Current @2.4 V	I_{OH}	−1.0			mA	
Output Current @0.4 V	I_{OL}	4.0			mA	

NOTES:

1. CLKX = CLKY = 1.544 MHz; MCLK = 10 MHz.

2. Outputs open; inputs swinging full supply levels.

3. Both channels in idle mode.

4. XOUT and YOUT when tristated.

PCM INTERFACE
A.C. ELECTRICAL CHARACTERISTICS

(0 °C to 70 °C, V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
MCLK Period	t_{PM}		100		ns	5
MCLK Pulse Width	t_{WMH}, t_{WML}	45	50	55	ns	
MCLK Rise and Fall Times	t_{RM}, t_{FM}		5	10	ns	
CLKX, CLKY Period	t_{PXY}	244	488	5208	ns	4
CLKX, CLKY Pulse Width	t_{WXYH}, t_{WXYL}	100	244		ns	
CLKX, CLKY Rise and Fall Times	t_{RXY}, t_{FXY}		10	20	ns	
Hold Time from CLKX, CLKY to FSX, FSY	t_{HOLD}	0			ns	1
Set-Up Time from FSX, FSY to CLKX, CLKY low	t_{SF}	50			ns	1
Hold Time from CLKX, CLKY low to FSX, FSY Low	t_{HF}	100			ns	1
XIN, YIN Set Up to CLKX, CLKY Low	t_{SD}	50			ns	1
XIN, YIN Hold to CLKX, CLKY Low	t_{HD}	50			ns	1
Delay Time from CLKX, CLKY to Valid XOUT, YOUT	t_{DXYO}	10		150	ns	2
Delay Time from CLKX, CLKY to XOUT, YOUT Tristated	t_{DXYZ}	20		150	ns	1,2,3

NOTES:

1. Measured at V_{IH} = 2.0V, V_{IL} = 0.8 V, and 10 ns maximum rise and fall times.

2. Load = 150 pF + 2 LSTTL loads.

3. For LSB of PCM byte or ADPCM nibble.

4. Maximum width of FSX, FSY is one CLKX, CLKY period.

5. MCLK = 10MHz ± 500ppm.

MASTER CLOCK/RESET
A.C. ELECTRICAL CHARACTERISTICS

(0 °C to 70 °C, V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
MCLK Period	t_{PM}		100		ns	5
MCLK Pulse Width	t_{WMH}, t_{WML}	45	50	55	ns	
$\overline{RST}$ Pulse Width	t_{WRL}		1		ms	

SERIAL PORT
A.C. ELECTRICAL CHARACTERISTICS

(0 °C to 70 °C, V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SDI to SCLK Set Up	t_{DC}	55			ns	1
SCLK to SDI Hold	t_{CDH}	55			ns	1
SCLK Low Time	t_{CL}	250			ns	1
SCLK High Time	t_{CH}	250			ns	1
SCLK Rise and Fall Times	t_R, t_F			100	ns	1
$\overline{CS}$ to SCLK Set Up	t_{CC}	50			ns	1
SCLK to $\overline{CS}$ Hold	t_{CCH}	250			ns	1
$\overline{CS}$ Inactive Time	t_{CWH}	250			ns	1
SCLK Set Up to $\overline{CS}$ Falling	t_{SCC}	50			ns	1

NOTES:
1. Measured at V_{IH} = 2.0V, V_{IL} = 0.8V, and 10 ns maximum rise and fall times.
5. MCLK = 10MHz ± 500ppm.

PCM INTERFACE A.C. TIMING DIAGRAM Figure 11
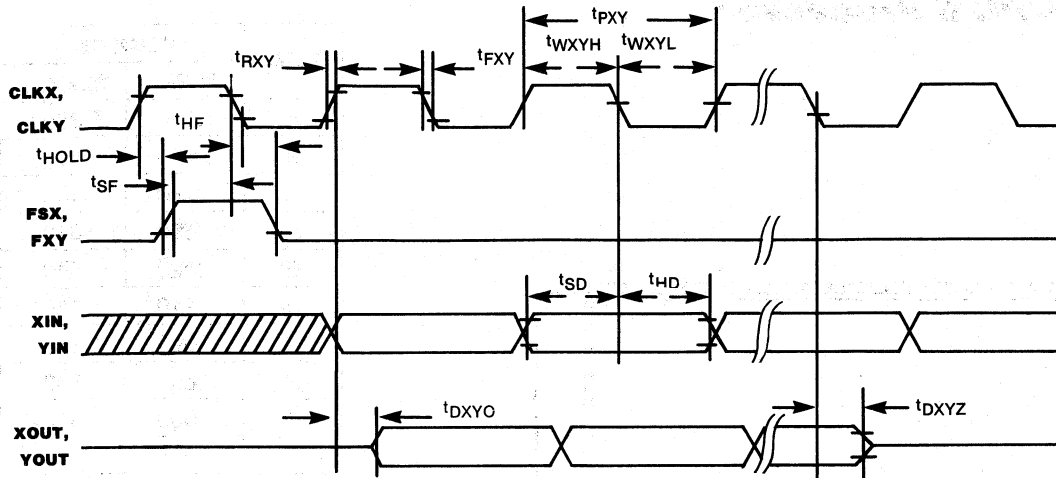
MASTER CLOCK/RESET A.C. TIMING DIAGRAM Figure 12
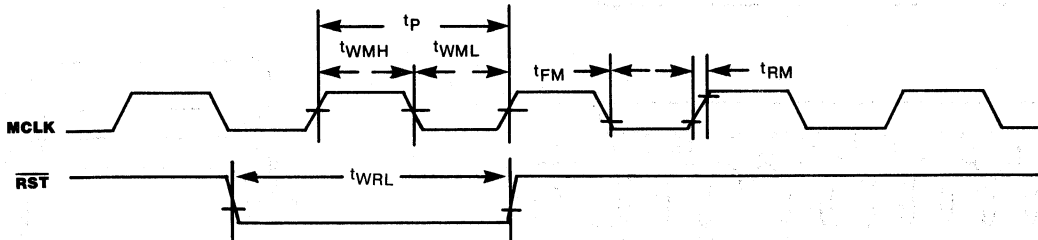
SERIAL PORT WRITE A.C. TIMING DIAGRAM Figure 13
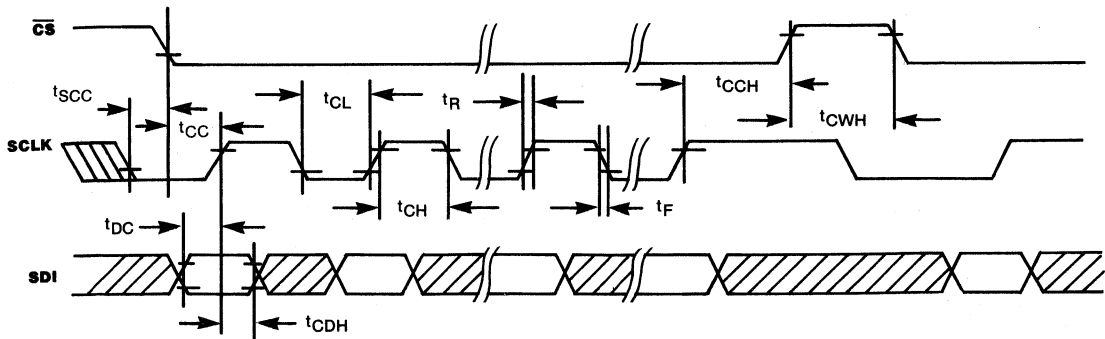
DS2167/68
ADPCM Processor

DIM.	INCHES	
	MIN.	MAX.
A	1.240	1.280
B	.540	.560
C	.140	.160
D	.590	.610
E	.020	.040
F	.110	.130
G	.090	.110
H	.600	.680
J	.008	.012
K	.015	.021

11 Equal Spaces at
.100 ± .010 TNA
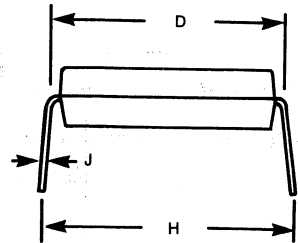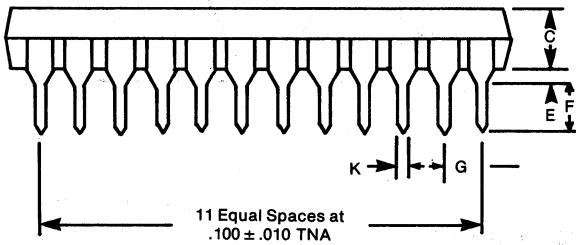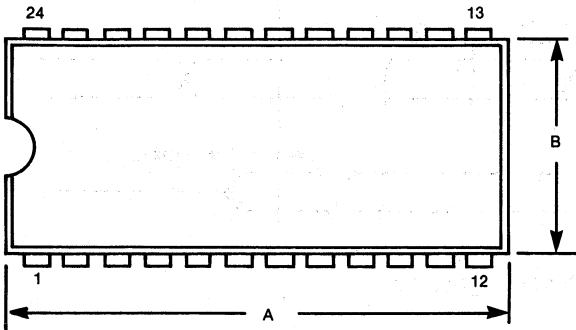
DS2167/68Q
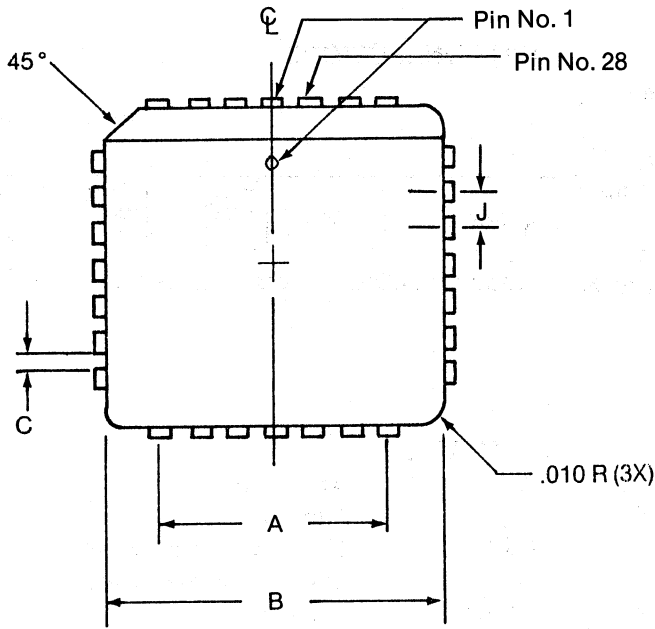
DIM.	INCHES	
	MIN.	MAX.
A	.290	.310
B	.441	.451
C	.020	.024
D	.018	.022
E	.488	.492
F	.118	.122
G	.020	.030
H	.390	.430
J	.048	.052

2

Dallas Semiconductor
ADPCM SipStik
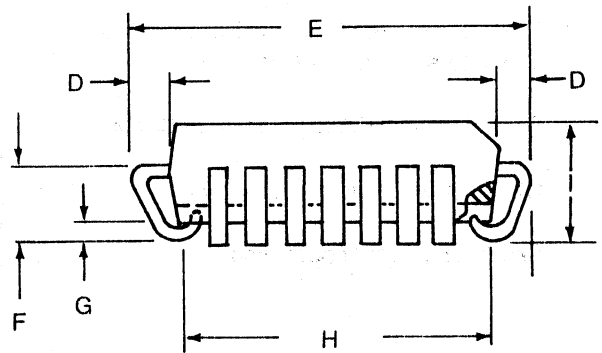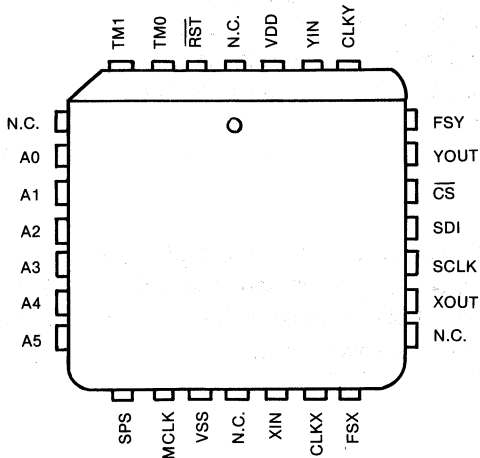
FEATURES

● 4 or 8 channels of full duplex operation

● Can be cascaded in multiples of 4 or 8
  channels for a maximum of 64 total channels

● Based on the DS2167 ADPCM processor
  which meets T1Y1 recommendations and the
  "new" CCITT G.721 recommendation

● Dual PCM highway architecture with
  programmable TSACs

● Simple serial port interfaces to a
  microprocessor; used to assign timeslots
  and control processing

● On-board buffers for all critical signals and
  capacitors for decoupling

● Conforms to JEDEC 35-position SIMM

● CMOS processors for low power consumption

● Single +5V supply operation

PIN CONNECTIONS
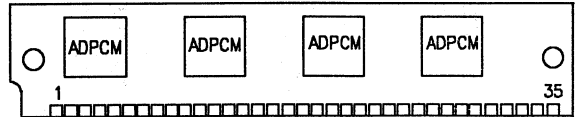
PIN NAMES

V_{DD}	+5V Supply
V_{SS}	Ground
A2HI	Higher 4-channel select
A2LO	Lower 4-channel select
A3-A5	Card Address
RST	Reset
SDI	Serial Data Input
SCLK	Serial Clock
CS	Chip Select
MCLK	10 MHz clock
XIN, YIN	Data Input
XOUT, YOUT	Data Output
FSX, FSY	Frame Syncs
CLKX, CLKY	Clocks for Data

DESCRIPTION

The DS2264 (4-channel) and DS2268 (8-chan-
nel) use the DS2167 in a surface mount package
to achieve a high density ADPCM array. The
ADPCM SipStiks can be connected in parallel to
obtain 64 channels of full duplex operation. For
component information, see the DS2167 data
sheet. For detailed product information, contact
your local sales office.

Voice/Data Encryption

Dallas Semiconductor
DES PROCESSOR

FEATURES

- Voice/data encryption chip compatible with the Data Encryption Standard (DES)

- Dual 64Kbps channel architecture - performs two encryptions, two decryptions, or in a full duplex fashion

- Interconnects directly with u-law or A-law combo-codec devices

- Supports three I/O data formats:

  - 8 bit per 8 KHz (standard)

  - 7 bit per 8 KHz (robbed bit signaling)

  - 4 bit per 8 KHz (32Kbps ADPCM)

- Serial PCM and control port interfaces minimize "glue" logic in multiple channel applications:

  - On-chip channel counters identify input and output time slots in TDM based systems

  - Unique addressing scheme simplifies device control; 3-wire port shared among up to 64 devices

- "Hardware" mode requires no host processor

- Available in 24-pin DIP and 28-pin PLCC

PIN CONNECTIONS

$\overline{RST}$	1	24	VDD
TM0	2	23	YIN
TM1	3	22	CLKY
A0	4	21	FSY
A1	5	20	YOUT
A2	6	19	$\overline{CS}$
A3	7	18	SDI
A4	8	17	SCLK
A5	9	16	XOUT
SPS	10	15	FSX
MCLK	11	14	CLKX
VSS	12	13	XIN
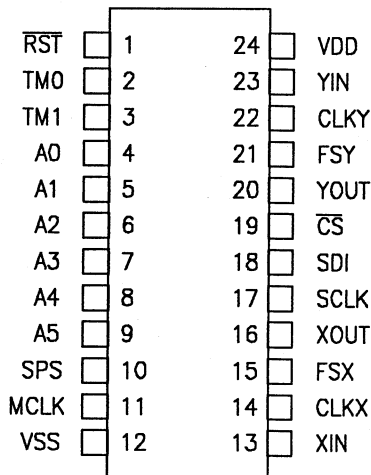
DESCRIPTION

The DS2160 is a programmable digital signal processing (DSP) CMOS chip with the Data Encryption Standard (DES) algorithm coded in firmware. The chip performs encipher/decipher operations on 64-bit words and uses a 64-bit key to provide security as specified by the DES. This algorithm is used in both governmental and commercial applications where sensitive information is passed through unsecured media.

4

Dallas Semiconductor
T1/CEPT Elastic Store

DS2175

FEATURES

- Rate buffer for T1 and CEPT transmission systems
- Synchronizes loop-timed and system-timed data streams on frame boundaries
- Ideal for T1 (1.544 MHz) to CEPT (2.048 MHz), CEPT to T1 interfaces
- Supports parallel and serial backplanes
- Buffer depth is 2 frames
- Comprehensive on-chip "slip" control logic
  - Slips occur only on frame boundaries
  - Outputs report slip occurrences and direction
  - Align feature allows buffer to be recentered at any time
  - Buffer depth easily monitored
- Compatible with DS2180A DS2181 CEPT Transceivers
- Industrial temperature range of −40° to +85°C available, designated DS2175IND

PIN CONNECTIONS

RCLKSEL	1	16	VDD
RCLK	2	15	SYSCLK
RSER	3	14	SSER
RMSYNC	4	13	SMSYNC
FSD	5	12	SFSYNC
$\overline{SLIP}$	6	11	SCHCLK
$\overline{ALN}$	7	10	S/$\overline{P}$
VSS	8	9	SCLKSEL
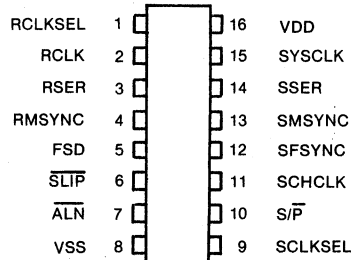
DESCRIPTION

The DS2175 is a low-power CMOS elastic-store memory optimized for use in primary rate telecommunications transmission equipment. The device serves as a synchronizing element between async data streams and is compatible with North American (T1—1.544 MHz) and European (CEPT—2.048 MHz) rate networks. The chip has several flexible operating modes which eliminate support logic and hardware currently required to interconnect parallel or serial TDM backplanes. Application areas include digital trunks, drop and insert equipment, digital cross-connects (DACS), private network equipment and PABX-to-computer interfaces such as DMI and CPI.

DS2175 BLOCK DIAGRAM Figure 1
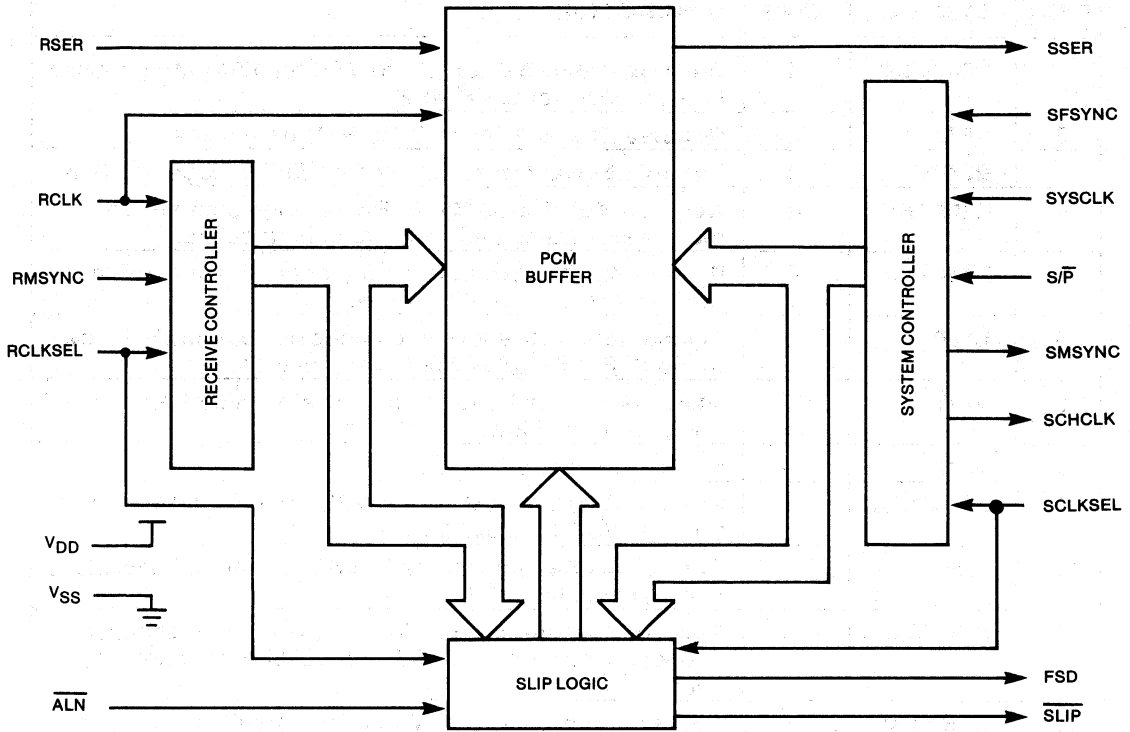
PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	RCLKSEL	I	**Receive Clock Select.** Tie to VSS for 1.544 MHz applications, to VDD for 2.048 MHz.
2	RCLK	I	**Receive Clock.** 1.544 or 2.048 MHz data clock.
3	RSER	I	**Receive Serial Data.** Sampled on falling edge of RCLK.
4	RMSYNC	I	**Receive Multiframe Sync.** Rising edge establishes receive side frame and multiframe boundaries.
5	FSD	O	**Frame Slip Direction.** State indicates direction of last slip; latched on slip occurrence.
6	SLIP	O	**Frame Slip.** Active low, open collector output. Held low for 65 SYSCLK cycles when a slip occurs.
7	ALN	I	**Align.** Recenters buffer on next system side frame boundary when forced low.
8	VSS	—	**Signal ground.** 0.0 volts.
9	SCLKSEL	I	**System Clock Select.** Tie to VSS for 1.544 MHz applications, to VDD for 2.048 MHz.
10	S/P̄	I	**Serial/Parallel Select.** Tie to VSS for parallel backplane applications, to VDD for serial.
11	SCHCLK	O	**System Channel Clock.** Transitions high on channel boundaries; useful for serial to parallel conversion of channel data.
12	SFSYNC	I	**System Frame Sync.** Rising edge establishes system side frame boundaries.
13	SMSYNC	O	**System Multiframe Sync.** Slip-compensated multiframe output; used with RMSYNC to monitor depth of store real time.
14	SSER	O	**System Serial Data.** Updated on rising edge of SYSCLK.
15	SYSCLK	I	**System Clock.** 1.544 or 2.048 MHz data clock.
16	VDD	—	**Positive Supply.** 5.0 volts.

PCM BUFFER

The DS2175 utilizes a 2-frame buffer to synchronize incoming PCM data to the system backplane clock. Buffer depth is mode-dependent; 2.048 MHz to 2.048 MHz applications utilize 64 bytes of buffer memory, while all other modes are supported by 48 bytes. The buffer samples data at RSER on the falling edge of RCLK. Output data appears at SSER and is updated on the rising edge of SYSCLK. The buffer depth is constantly monitored by on-board contention logic; a "slip" occurs when the buffer is completely emptied or filled. Slips automatically recenter the buffer to a one-frame depth and always occur on frame boundaries.

DATA FORMAT

Data is presented to, and output from, the elastic store in a "framed" format. A rising edge at RMSYNC and SFSYNC establishes frame boundaries for the receive and system sides. North American (T1) frames contain 24 data channels of 8 bits each and an F-bit (193 bits total). European (CEPT) frames contain 32 data channels (256 bits). The frame rate of both systems is 8 KHz. RMSYNC and SFSYNC do not require a pulse at every frame boundary; if desired, they may be pulsed once to establish frame alignment. Internal counters will then maintain the frame alignment and may be reinforced by the next rising edge at RMSYNC and/or SFSYNC.

SLIP CORRECTION CAPABILITY

The 2-frame buffer depth is adequate for T-carrier and CEPT applications where short term jitter synchronization, rather than correction of significant frequency differences, is required. The DS2175 provides an ideal balance between total delay (less than 250 microseconds at its full depth) and slip correction capability.

BUFFER RECENTERING

Many applications require that the buffer be recentered during system power-up and/or initialization. Forcing ALN low recenters the buffer on the next rising edge of SFSYNC. A slip will occur during this recentering if the buffer depth is adjusted. If the depth is presently optimum, no adjustment (slip) occurs.

SLIP REPORTING

SLIP is held low for 65 SYSCLK cycles when a slip occurs. SLIP is an active-low, open-collector output. FSD indicates slip direction. When low (buffer empty) a frame of data was "repeated" at SSER during the previous slip. When high (buffer full), a frame of data was "deleted." FSD is updated at every slip occurrence.

BUFFER DEPTH MONITORING

SMSYNC is a system side output pulse which indicates system side multiframe boundaries. The distance between rising edges of RMSYNC and SMSYNC indicates the current buffer depth. Impending slip conditions may be determined by monitoring RMSYNC and SMSYNC real time. SMSYNC is held high for 65 SYSCLK periods.

4

CLOCK SELECT
Receive and system side clock frequencies are independently selectable by inputs RCLKSEL and SCLKSEL. 1.544 MHz is selected when RCLKSEL (SCLKSEL) = 0; 2.048 MHz is selected when RCLKSEL (SCLKSEL) = 1. In 1.544 MHz (receive) to 1.544 MHz (system) applications, the F-bit position is passed through the receive buffer and presented at SSER immediately after a rising edge on SFSYNC. The F-bit position is forced to 1 in 2.048 MHz to 1.544 MHz applications. No F-bit position exists in 2.048 MHz system side applications.

PARALLEL COMPATIBILITY
The DS2175 is compatible with parallel and serial backplanes. Channel 1 data appears at SSER after a rising edge at SFSYNC (serial applications, S/$\overline{P}$ = 1). The device utilizes a look-ahead circuit in parallel applications (S/$\overline{P}$ = 0), and presents data 8 clocks early as shown in figures 4 and 5. Converting SSER to a parallel format requires an HC595 shift register.

RECEIVE SIDE TIMING (RCLK = 1.544 MHz) Figure 2
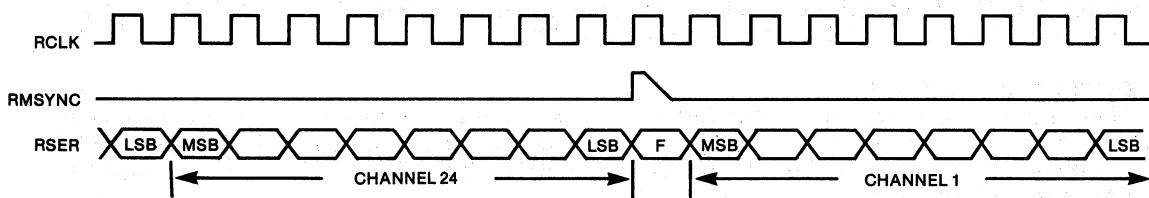
RECEIVE SIDE TIMING (RCLK = 2.048 MHz) Figure 3
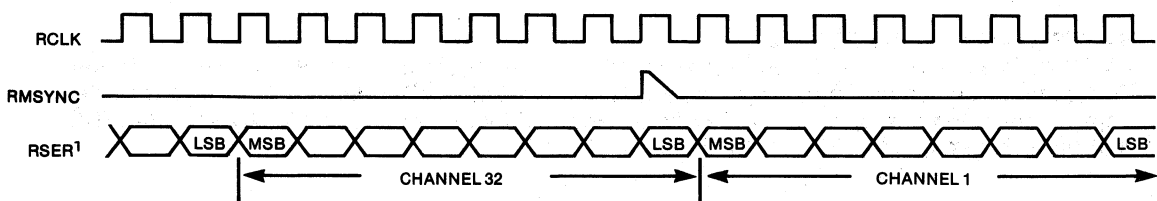
NOTES:
1. All channel data is passed through the elastic store in 2.048 MHz system side applications (SCLKSEL = 1); Data in channels > 24 is ignored in 1.544 MHz system side applications (SCLKSEL = 0).

SYSTEM MULTIFRAME BOUNDARY TIMING (SYSCLK = 1.544 MHz) Figure 4
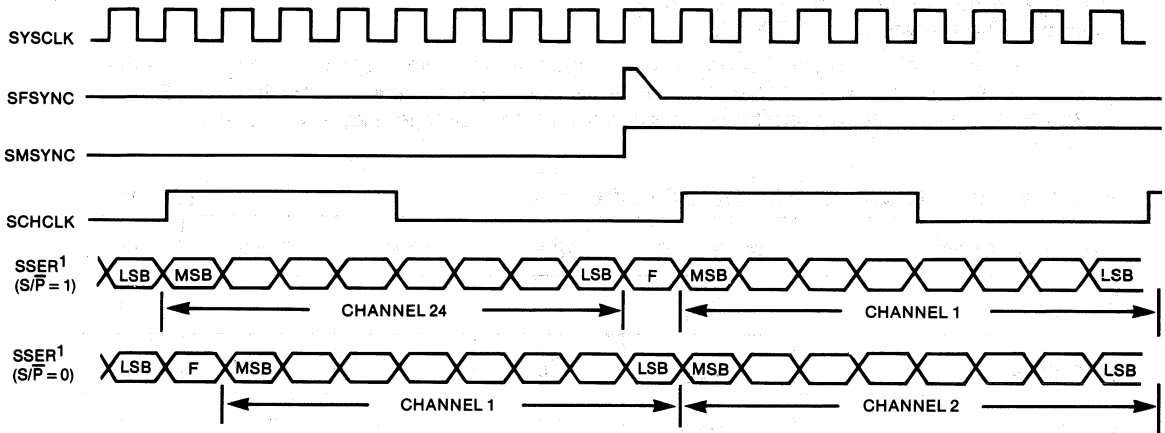
NOTES:
1. In 1.544 MHz receive side applications (RCLKSEL = 0), the F-bit position contains F-bit data extracted from the data stream at RSER. The F-bit position is forced to "1" in 2.048 MHz receive side applications (RCLKSEL = 1).

SYSTEM MULTIFRAME BOUNDARY TIMING (SYSCLK = 2.048 MHz) Figure 5
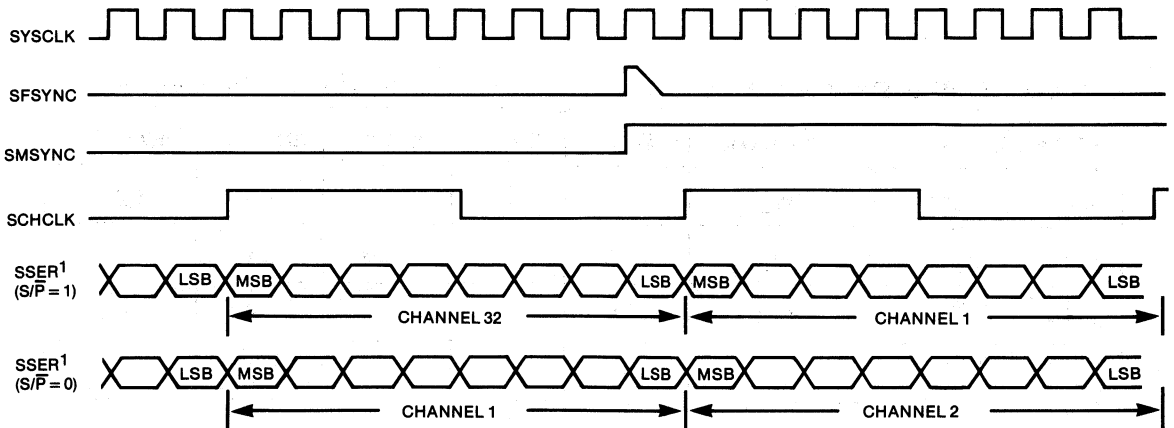
NOTES:
1. All channel data is passed through the elastic store in 2.048 MHz system side applications (SCLKSEL = 1); Data in channels > 24 is ignored in 1.544 MHz system side applications (SCLKSEL = 0).

ABSOLUTE MAXIMUM RATINGS*
Voltage on any Pin Relative to Ground $-1.0V$ to $+7.0V$
Operating Temperature   0 °C to 70 °C
Storage Temperature -55 °C to $+125$ °C
Soldering Temperature 260 °C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS   (0 °C to 70 °C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Logic 1	V_{IH}	2.0		$V_{DD}+0.3$	V
Logic 0	V_{IL}	-0.3		$+0.8$	V
Supply	V_{DD}	4.5		5.5	V

CAPACITANCE   ($t_A = 25$ °C)

PARAMETER	SYMBOL	MAX	UNITS
Input Capacitance	C_{IN}	5	pF
Output Capacitance	C_{OUT}	7	pF

D.C. ELECTRICAL CHARACTERISTICS   (0 °C to 70 °C $V_{DD} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		6		mA	1,2
Input Leakage	I_{IL}	-1.0		$+1.0$	uA	
Output Current @2.4V	I_{OH}	-1.0			mA	3
Output Current @0.4V	I_{OL}	$+4.0$			mA	4

NOTES:
1. SYSCLK = RCLK = 2.048 MHz

2. Outputs open

3. All outputs except $\overline{\text{SLIP}}$, which is open collector

4. All outputs

A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C, V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t_{RCLK}	200			ns	
RCLK, SYSCLK Rise and Fall Times	t_R, t_F			20	ns	
RCLK Pulse Width	t_{RWH}, t_{RWL}	100			ns	
SYSCLK Pulse Width	t_{SWH}, t_{SWL}	100			ns	
SYSCLK Period	t_{SYSCLK}	200			ns	
RMSYNC Setup to RCLK Rising	t_{SC}	$-t_{RWH}/2$		$+t_{RWL}/2$	ns	
SFSYNC Setup to SYSCLK Rising	t_{SC}	$-t_{SWH}/2$		$+t_{SWL}/2$	ns	
RMSYNC, SFSYNC, $\overline{ALN}$ Pulse Width	t_{PW}	100			ns	
RSER Set Up to RCLK Falling	t_{SD}	50			ns	
RSER Hold from RCLK Falling	t_{HD}	50			ns	
Propagation Delay SYSCLK to SSER	t_{PVD}			75	ns	
Propagation Delay SYSCLK to SMSYNC High	t_{PSS}			75	ns	
Propagation Delay SYSCLK or RCLK to $\overline{SLIP}$ Low, FSD LOW/HIGH	t_{PS}			100	ns	
$\overline{ALN}$ Set Up to SFSYNC Rising	t_{SR}	500			ns	

NOTES:

1. Measured at V_{IH} = 2.0V, V_{IL} = 0.8V, and 10 ns maximum rise and fall times

2. Output load capacitance = 100 pF

4

RECEIVE A.C. TIMING DIAGRAM Figure 6
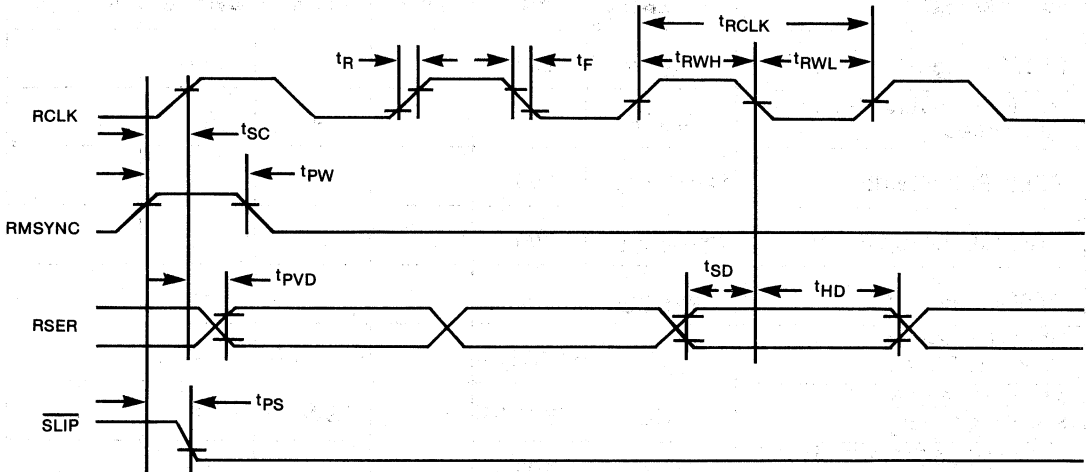
SYSTEM A.C. TIMING DIAGRAM Figure 7
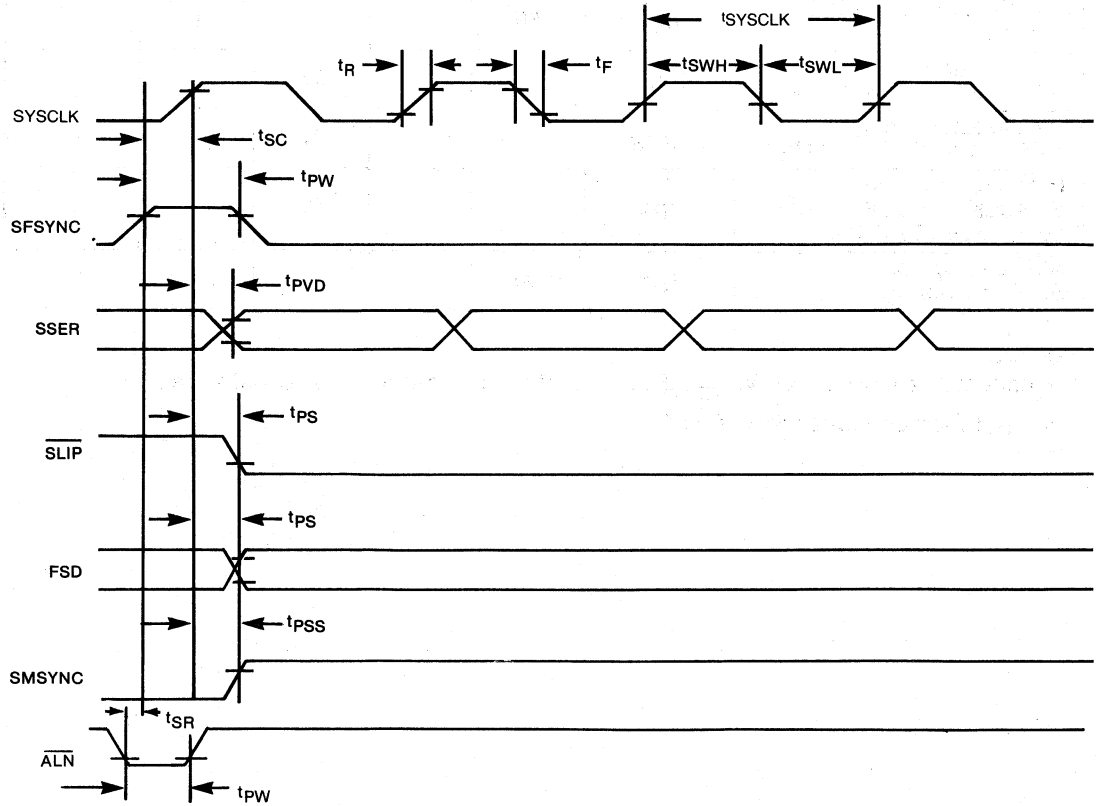
DS2175
T1/CEPT Elastic Store
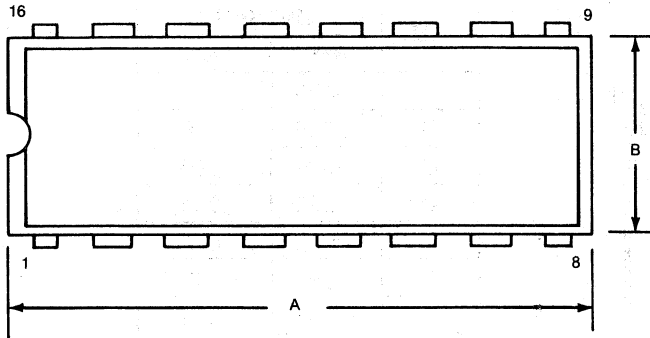
DIM.	INCHES	
	MIN.	MAX.
A	.740	.780
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.030
F	.110	.130
G	.090	.110
H	.300	.350
J	.008	.012
K	.015	.021

7 Equal Spaces at
.100 ± .010 (TNA)

4
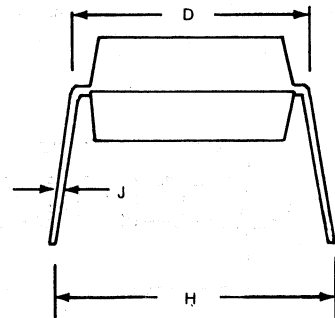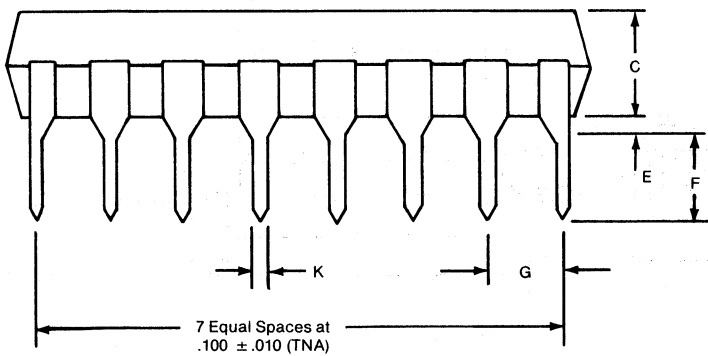
DS2175S
T1/CEPT Elastic Store
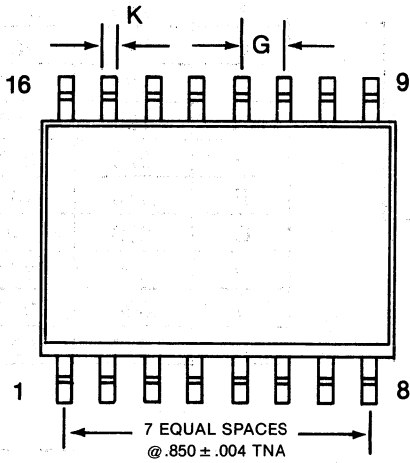
DIM.	INCHES	
	MIN.	MAX.
A	.403	.411
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019

7 EQUAL SPACES
@ .850 ± .004 TNA

6° TYP

Dallas Semiconductor
T1 Receive Buffer

DS2176
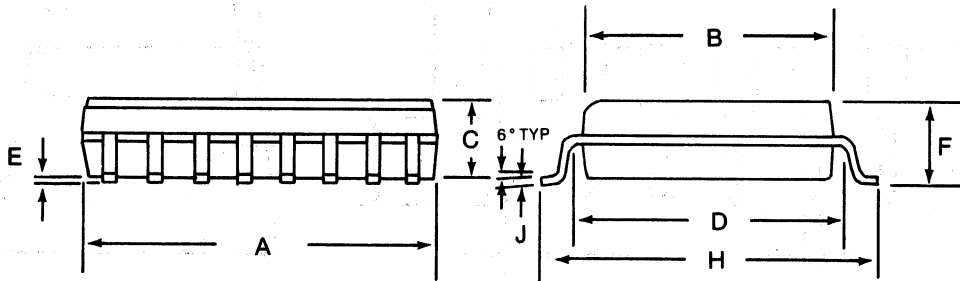
FEATURES

- Synchronizes loop-timed and system-timed T1 data streams
- Two-frame buffer depth; slips occur on frame boundaries
- Output indicates when slip occurs
- Buffer may be recentered externally
- Ideal for 1.544 to 2.048 MHz rate conversion
- Interfaces to parallel or serial backplanes
- Extracts and buffers robbed-bit signalling
- Inhibits signalling updates during alarm or slip conditions
- Integration feature "debounces" signalling
- Slip-compensated output indicates when signalling updates occur
- Compatible with DS2180A T1 Transceiver
- Surface mount package available, designated DS2176Q
- Industrial temperature range of −40°C to +85°C available, designated DS2176IND

PIN CONNECTIONS

$\overline{\text{SIGH}}$	1	24	VDD
RMSYNC	2	23	SCLKSEL
RCLK	3	22	SYSCLK
RSER	4	21	SSER
A	5	20	$\overline{\text{SLIP}}$
B	6	19	SBIT8
C	7	18	SMSYNC
D	8	17	SIGFRZ
SCHCLK	9	16	SFSYNC
SM0	10	15	$\overline{\text{ALN}}$
SM1	11	14	FMS
VSS	12	13	$S/\overline{P}$

4
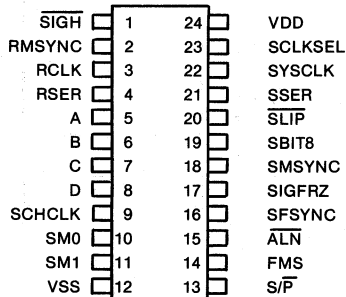
DESCRIPTION

The DS2176 is a low-power CMOS device specifically designed for synchronizing receive side loop-timed T-carrier data streams with system side timing. The device has several flexible operating modes which simplify interfacing incoming data to parallel and serial TDM backplanes. The device extracts, buffers and integrates ABCD signalling; signalling updates are prohibited during alarm or slip conditions. The buffer replaces extensive hardware in existing applications with one "skinny" 24-lead package. Application areas include digital trunks, drop and insert equipment, transcoders, digital cross-connects (DACS), private network equipment and PABX-to-computer interfaces such as DMI and CPI.

DS2176 BLOCK DIAGRAM Figure 1
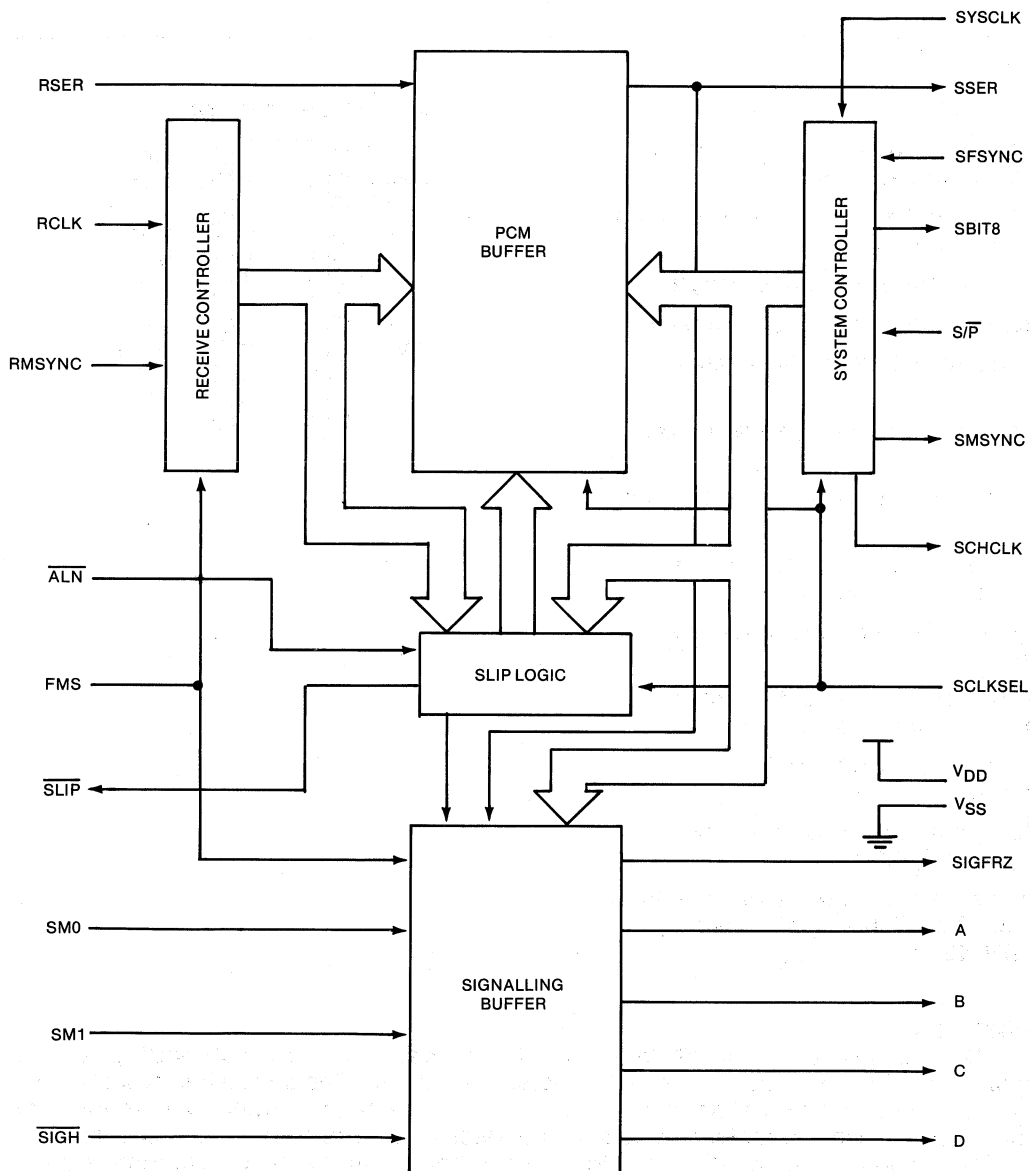
PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	$\overline{\text{SIGH}}$	I	**Signalling Inhibit.** When low, ABCD signalling updates are disabled for a period determined by SM0 and SM1, or until returned high.
2	RMSYNC	I	**Receive Multiframe Sync.** Must be pulsed high at multiframe boundaries to establish frame and multiframe alignment.
3	RCLK	I	**Receive Clock.** Primary 1.544 MHz clock.
4	RSER	I	**Receive Serial Data.** Sampled on falling edge of RCLK.
5 6 7 8	A B C D	O	**Robbed-Bit Signalling Outputs**
9	SCHCLK	O	**System Channel Clock.** Transitions high on channel boundaries; useful for serial to parallel conversion of channel data.
10 11	SM0 SM1	I	**Signalling Modes 0 and 1.** Select signalling supervision technique.
12	VSS	—	**Signal ground.** 0.0 volts.
13	$\text{S}/\overline{\text{P}}$	I	**Serial/Parallel Select.** Tie to VSS for parallel backplane applications, to VDD for serial.
14	FMS	I	**Frame Mode Select.** Tie to VSS to select 193S (D4) framing, to VDD for 193E (extended).
15	$\overline{\text{ALN}}$	I	**Align.** Recenters buffer on next system side frame boundary when forced low.
16	SFSYNC	I	**System Frame Sync.** Rising edge establishes start of frame.
17	SIGFRZ	O	**Signalling Freeze.** When high, indicates signalling updates have been disabled internally via a slip or externally by forcing $\overline{\text{SIGH}}$ low.
18	SMSYNC	O	**System Multiframe Sync.** Slip-compensated multiframe output; indicates when signalling updates are made.
19	SBIT8	O	**System Bit 8.** High during the LSB time of each channel. Used to reinsert extracted signalling into outgoing data stream.

4

20	SLIP	O	**Frame Slip.** Active low, open collector output. Held low for 64 SYSCLK cycles when a slip occurs.
21	SSER	O	**System Serial Out.** Updated on rising edge of SYSCLK.
22	SYSCLK	I	**System Clock.** 1.544 or 2.048 MHz data clock.
23	SCLKSEL	I	**System Clock Select.** Tie to VSS for 1.544 MHz applications, to VDD for 2.048 MHz.
24	VDD	—	**Positive Supply.** 5.0 volts.

OVERVIEW

The DS2176 performs two primary functions: 1) *synchronization* of received T1 PCM data (looped timed) to host backplane frequencies; 2) *supervision* of robbed-bit signalling data embedded in the data stream. The buffer, while optimized for use with the DS2180A T1 Transceiver, is also compatible with other transceiver devices. The DS2180A data sheet should serve as a valuable reference when designing with the DS2176.

RECEIVE SIDE TIMING Figure 2
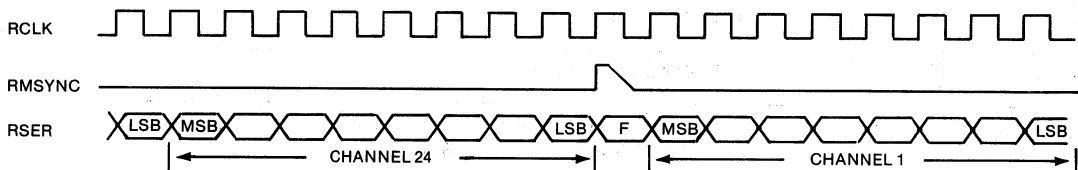
DATA SYNCHRONIZATION

PCM BUFFER
The DS2176 utilizes a 2-frame buffer (386 bits) to synchronize incoming PCM data to the system backplane clock. The buffer samples data at RSER on the falling edge of RCLK. Output data appears at SSER and is updated on the rising edge of SYSCLK. A rising edge at RMSYNC establishes receive side frame and multiframe alignment. A rising edge at SFSYNC establishes system side frame alignment. The buffer depth is constantly monitored by on-board contention logic, a "slip" occurs when the buffer is completely emptied or filled. Slips automatically recenter the buffer to a one-frame depth and always occur on frame boundaries.

SLIP CORRECTION CAPABILITY
The 2-frame buffer depth is adequate for most T-carrier applications where short-term jitter synchronization, rather than correction of significant frequency differences, is required. The DS2176 provides an ideal balance between total delay and slip correction capability.

BUFFER RECENTERING
$\overline{SLIP}$ is held low for 65 SYSCLK cycles when a slip occurs. $\overline{SLIP}$ is an active-low, open-collector output.

BUFFER DEPTH MONITORING
SMSYNC is a system side output pulse which indicates system side multiframe boundaries. The distance between rising edges at RMSYNC and SMSYNC indicates the current buffer depth. Slip direction and/or an impending slip condition may be determined by monitoring RMSYNC and SMSYNC real time. SMSYNC is held high for 65 SYSCLK cycles.

CLOCK SELECT
The device is compatible with 2 common backplane frequencies: 1.544 MHz, selected when SCLKSEL = 0; and 2.048 MHz, selected when SCLKSEL = 1. In 1.544 MHz applications the F-bit is passed through the receive buffer and presented at SSER immediately after a rising edge on SFSYNC. The F-bit is dropped in 2.048 MHz applications and the MSB of channel 1 appears at SSER one bit period after a rising edge at SFSYNC. SSER is forced to 1 in all channels greater than 24. See figures 3 and 4.

In 2.048 MHz applications (SCLKSEL = 1), the PCM buffer control logic establishes slip criteria different from that used in 1.544 MHz applications to compensate for the faster system-side read frequency.

PARALLEL COMPATIBILITY
The DS2176 is compatible with parallel and serial backplanes. Channel 1 data appears at SSER after a rising edge at SFSYNC as shown in figures 3 and 4 (serial applications, S/$\overline{P}$ = 1). The device utilizes a look-ahead circuit in parallel applications (S/$\overline{P}$ = 0). Data is output 8 clocks earlier, allowing the user to parallel convert data externally.

SYSTEM MULTIFRAME BOUNDARY TIMING (SYSCLK = 1.544 MHZ) Figure 3
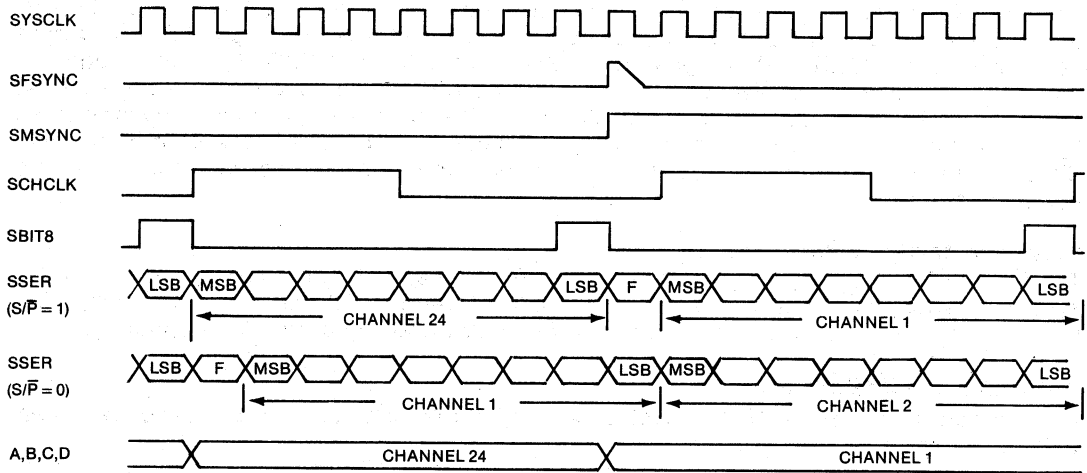
SYSCLK
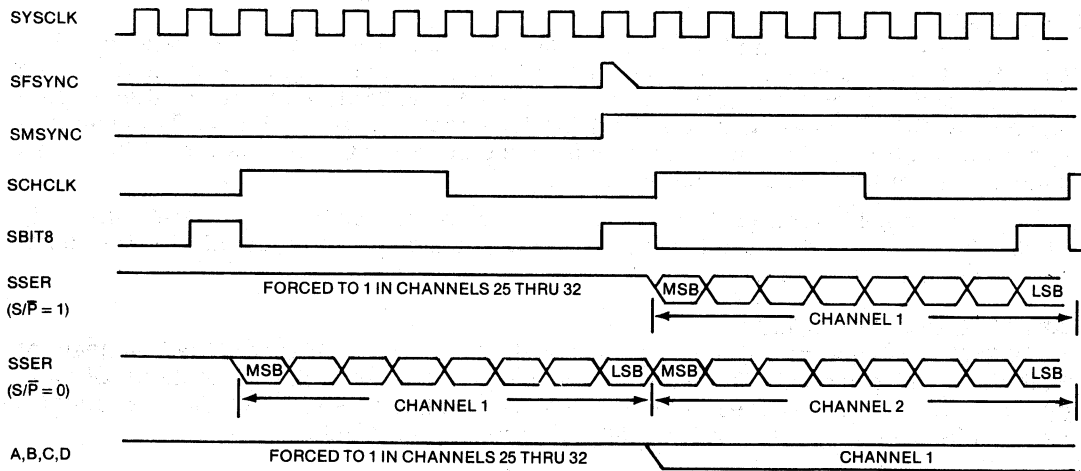
SFSYNC

SMSYNC

SCHCLK

SBIT8

SSER
(S/$\overline{P}$ = 1)

LSB MSB LSB F MSB LSB
CHANNEL 24 CHANNEL 1

SSER
(S/$\overline{P}$ = 0)

LSB F MSB LSB MSB LSB
CHANNEL 1 CHANNEL 2

A,B,C,D

CHANNEL 24 CHANNEL 1

SYSTEM MULTIFRAME BOUNDARY TIMING (SYSCLK = 2.048 MHZ) Figure 4

SYSCLK

SFSYNC

SMSYNC

SCHCLK

SBIT8

SSER
(S/$\overline{P}$ = 1)

FORCED TO 1 IN CHANNELS 25 THRU 32 MSB LSB
CHANNEL 1

SSER
(S/$\overline{P}$ = 0)

MSB LSB MSB LSB
CHANNEL 1 CHANNEL 2

A,B,C,D

FORCED TO 1 IN CHANNELS 25 THRU 32 CHANNEL 1

193S SYSTEM MULTIFRAME TIMING Figure 5

FRAME # | 12 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 |

SFSYNC

SMSYNC

193E SYSTEM MULTIFRAME TIMING Figure 6

FRAME # | 24 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 1 |

SFSYNC

SMSYNC
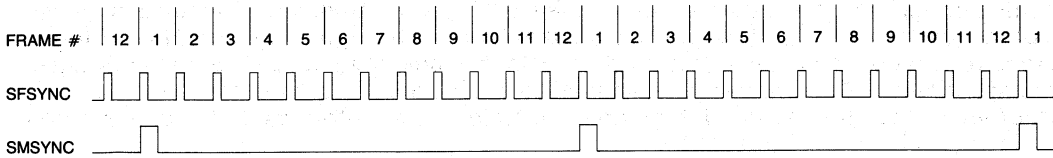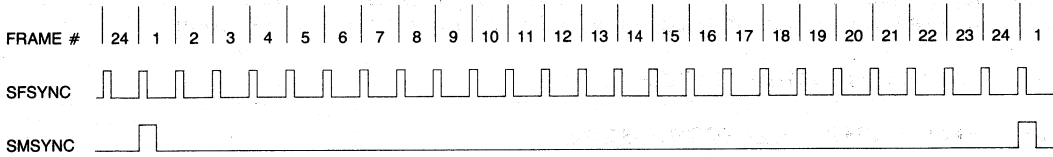
4

SIGNALLING SUPERVISION

EXTRACTION

In digital channel banks, robbed-bit signalling data is inserted into the LSB position of each channel during signalling frames. In 193S framing (FMS = 0) applications, A signalling data is inserted into frame 6 and B signalling data is inserted into frame 12. 193E framing (FMS = 1) includes 2 additional signalling bits: C signalling is inserted into frame 18 and D signalling is inserted into frame 24. This embedded signalling data is synchronized to system side timing (via the PCM buffer) before being extracted and presented at outputs A,B,C and D. Outputs A,B,C and D are valid for each individual channel time and are repeated per channel for all frames of the multiframe. In 193S applications, outputs C and D contain the previous multiframe's A and B data. Signalling updates occur once per multiframe at the rising edge of SMSYNC unless prohibited by a freeze.

FREEZE

The signalling buffer allows the DS2176 to "freeze" (prevent update of) signalling information during alarm or slip conditions. A slip condition or forcing SIGH low freezes signalling; duration of the freeze is dependent on SM0 and SM1. Updates will be unconditionally prohibited when SIGH is held low. During freezing conditions "old" data is recirculated in the output registers and appears at A,B,C and D. SIGFRZ is held high during the freeze condition, and returns low on the next signalling update. Input to output delay of signalling data is equal to 1 multiframe (the depth of the signalling buffer) + the current depth of the PCM buffer (1 frame ± approximately 1 frame).

INTEGRATION

Signalling integration is another feature of the DS2176; when selected, it minimizes the impact of random noise hits on the span and resultant robbed-bit signalling corruption. Integration requires that per-channel signalling data be in the same state for 2 or more multiframes before appearing at A,B,C and D. SM0 and SM1 are used to select the degree of integration or to totally bypass the feature. Integration is limited to 2 multiframes during slip or alarm conditions to minimize update delay.

CLEAR CHANNEL CONSIDERATIONS

The DS2176 does not merge the "processed" signalling information with outgoing PCM data at SSER; this assures integrity of data in clear channel applications. SBIT8 indicates the LSB position of each channel; when combined with off-chip support logic, it allows the user to selectively re-insert robbed-bit signalling data into the outgoing data stream.

SIGNALLING SUPERVISION MODES Table 2

SM0	SM1	FMS	SELECTED MODE
0	0	0	193S framing, no integration, 1 multiframe freeze.
0	0	1	193E framing, no integration, 1 multiframe freeze.
0	1	0	193S framing, 2 multiframes integration and freeze.
0	1	1	193E framing, 2 multiframes integration and freeze.
1	0	0[1]	193S framing, 5 multiframes integration, 2 multiframes freeze.
1	0	1[1]	193E framing, 3 multiframes integration, 2 multiframes freeze.
1	1	0	Test mode.
1	1	1	Test mode.

NOTES:
1. During slip or alarm conditions, integration is limited to 2 multiframes to minimize signalling delay.

SLIP AND SIGNALLING SUPERVISION LOGIC TIMING Figure 7
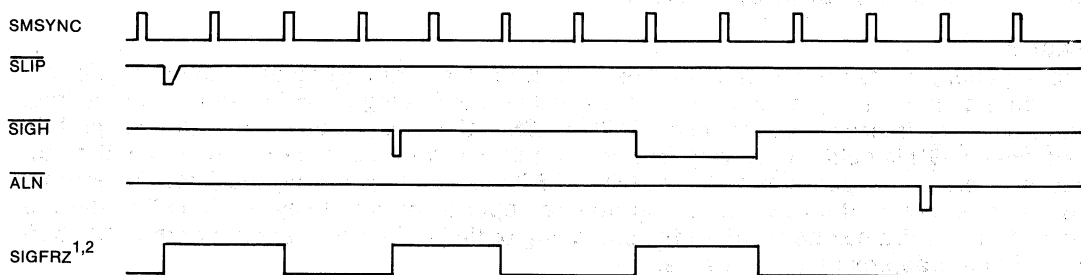
NOTES:
1. Integration feature disabled (SM0 = SM1 = 0) in timing set shown.
2. Depending on present buffer depth, forcing $\overline{ALN}$ low may or may not cause a slip condition.

SERIAL 1.544 MHZ BACKPLANE INTERFACE Figure 8
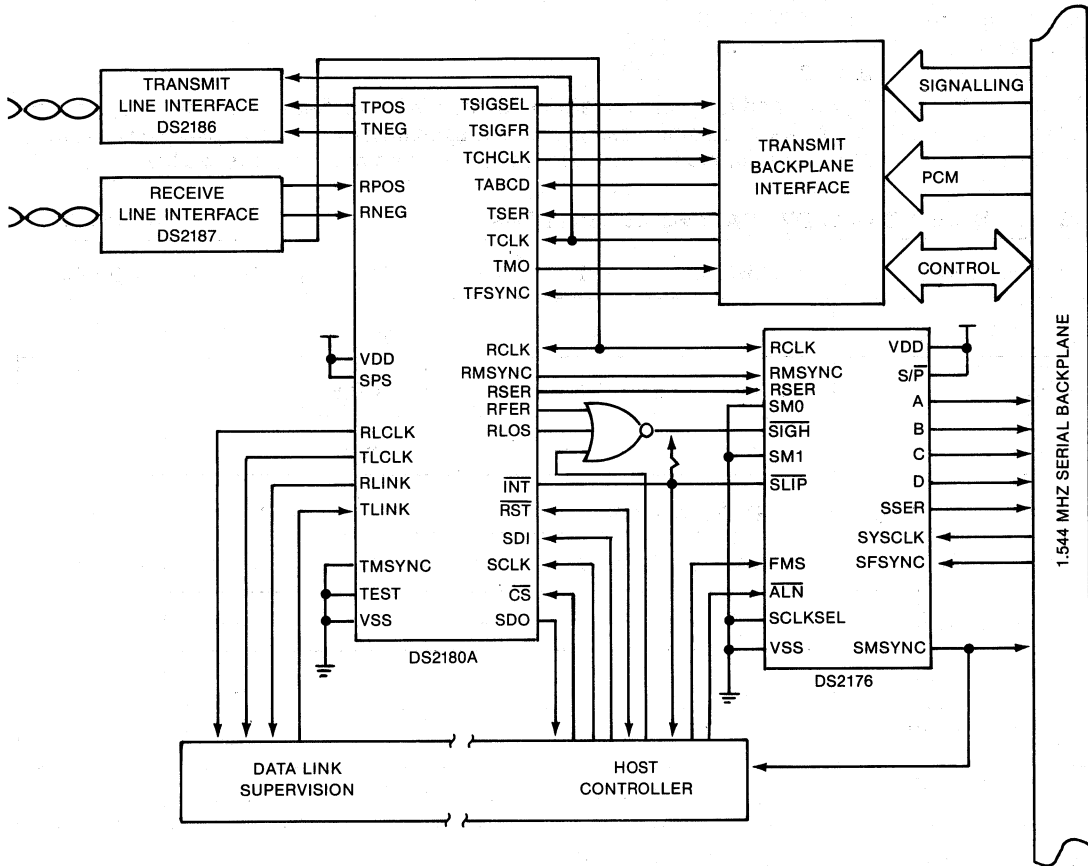
DS2176/DS2180A SYSTEM APPLICATION
Figure 8 shows how the DS2180A T1 Transceiver and DS2176 Receive Buffer interconnect in a typical application.

ABSOLUTE MAXIMUM RATINGS *

Voltage on any Pin Relative to Ground -1.0V to $+7.0$V
Operating Temperature   0 °C to 70 °C
Storage Temperature -55 °C to $+125$ °C
Soldering Temperature   260 °C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS   (0 °C to 70 °C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{DD} + 0.3$	V	
Logic 0	V_{IL}	-0.3		$+0.8$	V	
Supply	V_{DD}	4.5		5.5	V	

D.C. ELECTRICAL CHARACTERISTICS   (0 °C to 70 °C $V_{DD} = 5$V $\pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		6	10	mA	1,2
Input Leakage	I_{IL}	-1.0		$+1.0$	uA	
Output Current @2.4V	I_{OH}	-1.0			mA	3
Output Current @0.4V	I_{OL}	$+4.0$			mA	4
Output Leakage	I_{LO}	-1.0		$+1.0$	uA	5

NOTES:
1. TCLK = RCLK = 1.544 MHz
2. Outputs open
3. All outputs except $\overline{\text{SLIP}}$, which is open collector
4. All outputs
5. Applies to $\overline{\text{SLIP}}$ when tri-stated

CAPACITANCE $(t_A = 25\,°C)$

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

A.C. ELECTRICAL CHARACTERISTICS $(0\,°C \text{ to } 70\,°C, V_{DD} = 5V \pm 10\%)$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t_{RCLK}	250	648		ns	
RCLK, SYSCLK Rise and Fall Times	t_R, t_F			20	ns	
RCLK Pulse Width	t_{RWH}, t_{RWL}	125	324		ns	
SYSCLK Pulse Width	t_{SWH}, t_{SWL}	100	244		ns	
SYSCLK Period	t_{SYSCLK}	200	488		ns	
RMSYNC Setup to RCLK Rising	t_{SC}	$-t_{RWH}/2$		$+t_{RWL}/2$	ns	
SFSYNC Setup to SYSCLK Rising	t_{SC}	$-t_{SWH}/2$		$+t_{SWL}/2$	ns	
RMSYNC, SFSYNC, $\overline{SIGH}$ ALN Pulse Width	t_{PW}	100			ns	
RSER Setup to RCLK Falling	t_{SD}	50			ns	
RSER Hold from RCLK Falling	t_{HD}	50			ns	
Propagation Delay SYSCLK to SSER, A,B,C,D	t_{PVD}			100	ns	
Propagation Delay SYSCLK to SMSYNC High	t_{PSS}			75	ns	
Propagation Delay SYSCLK or RCLK to $\overline{SLIP}$ Low	t_{PS}			100	ns	
Propagation Delay SYSCLK to SIGFRZ Low/High	t_{PSF}			75	ns	
$\overline{ALN}$, $\overline{SIGH}$ Setup to SFSYNC Rising	t_{SR}	500			ns	

NOTES:
1. Measured at $V_{IH} = 2.0V$, $V_{IL} = 0.8V$, and 10 ns maximum rise and fall times.
2. Output load capacitance = 100 pF.

RECEIVE A.C. DIAGRAM Figure 9
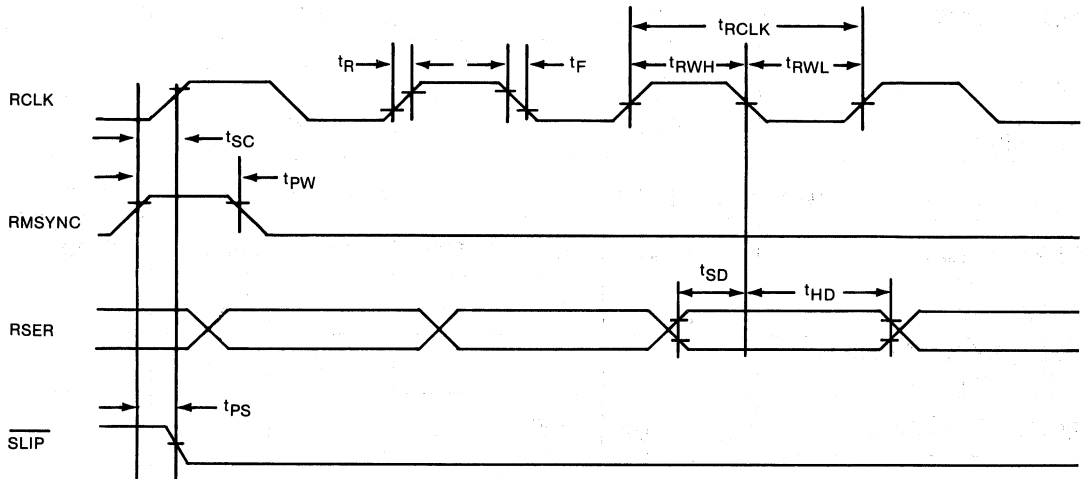
SYSTEM A.C. TIMING DIAGRAM Figure 10
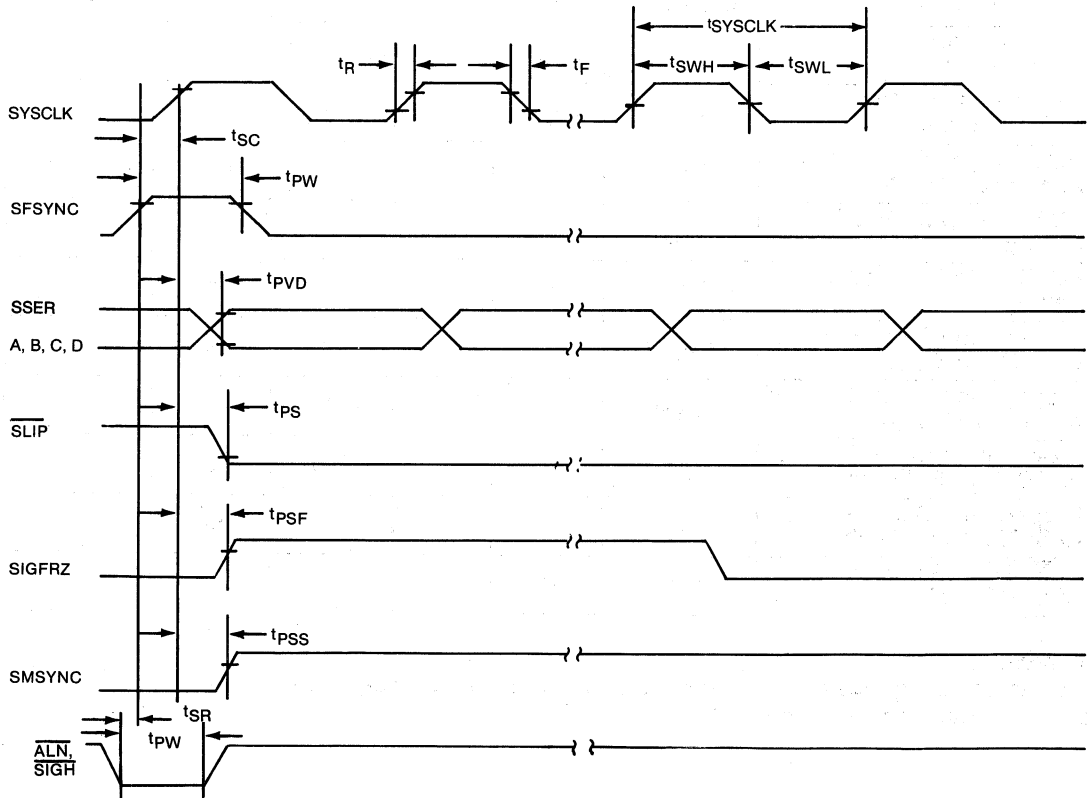
DS2176
T1 Receive Buffer
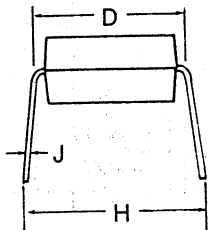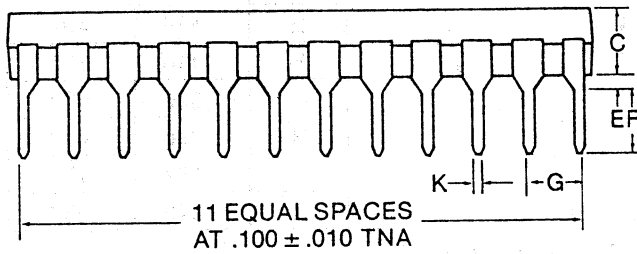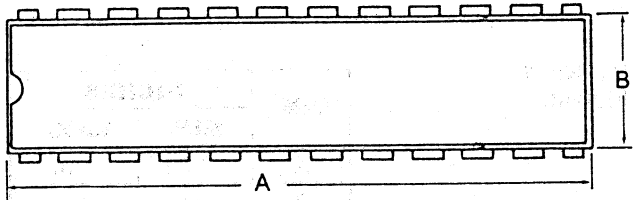
DIM.	INCHES	
	MIN.	MAX.
A	1.150	1.190
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.040
F	.110	.130
G	.090	.110
H	.325	.375
J	.008	.012
K	.015	.021

11 EQUAL SPACES
AT .100 ± .010 TNA

4

DS2176Q
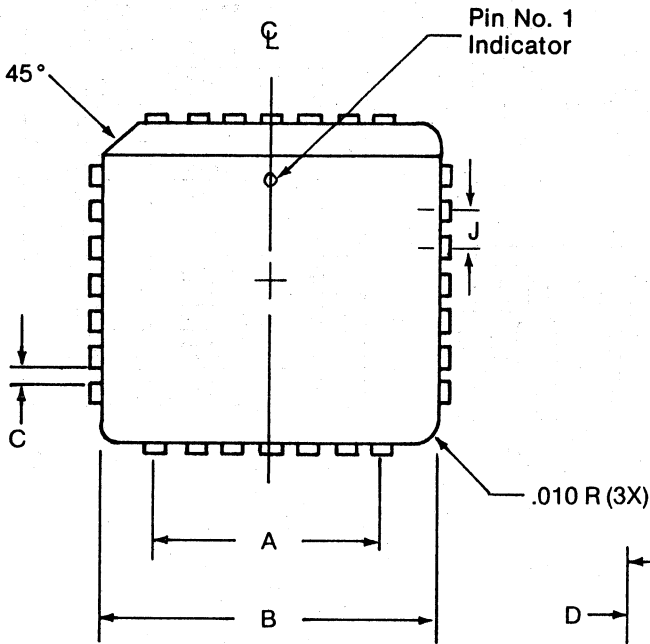
DIM.	INCHES	
	MIN.	MAX.
A	.290	.310
B	.441	.451
C	.020	.024
D	.018	.022
E	.488	.492
F	.118	.122
G	.020	.030
H	.390	.430
I	.167	.173
J	.048	.052

Transceivers/Framers

Dallas Semiconductor
T1 Transceiver

DS2180A
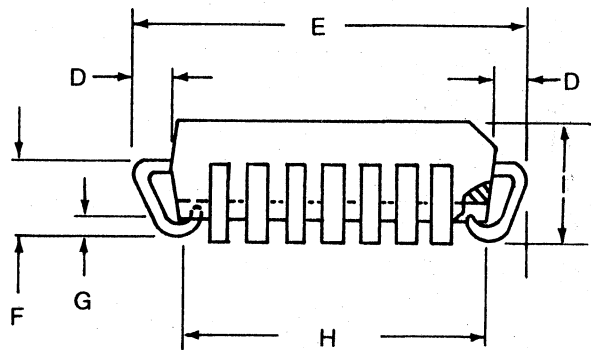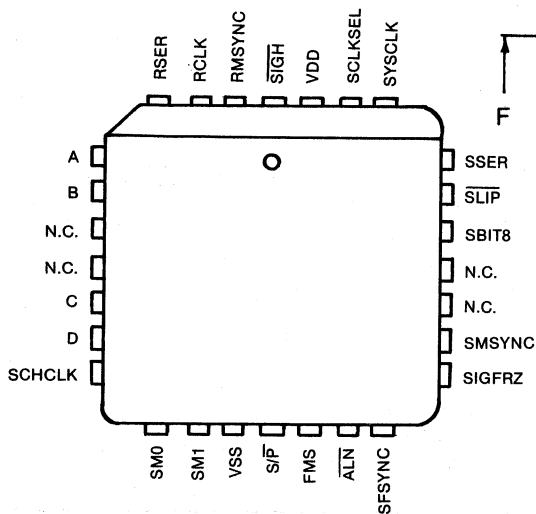
FEATURES

- Single chip DS1 rate transceiver
- Supports common framing standards
  - 12 frames/superframe "193S"
  - 24 frames/superframe "193E"
- Three zero suppression modes
  - B7 stuffing
  - B8ZS
  - Transparent
- Simple serial interface used for configuration, control and status monitoring in "processor" mode
- "Hardware" mode requires no host processor; intended for stand-alone applications
- Selectable 0, 2, 4, 16 state robbed bit signaling modes
- Allows mix of "clear" and "non-clear" DS0 channels on same DS1 link
- Alarm generation and detection
- Receive error detection and counting for transmission performance monitoring
- 5V supply, low power CMOS technology
- Surface mount package available, designated DS2180AQ
- Industrial temperature range of −40 °C to +85 °C available, designated DS2180AN or DS2180AQN

PIN CONNECTIONS

Pin	Signal		Pin	Signal
1	TMSYNC		40	VDD
2	TFSYNC		39	RLOS
3	TCLK		38	RFER
4	TCHCLK		37	RBV
5	TSER		36	RCL
6	TMO		35	RNEG
7	TSIGSEL		34	RPOS
8	TSIGFR		33	RST
9	TABCD		32	TEST
10	TLINK		31	RSIGSEL
11	TLCLK		30	RSIGFR
12	TPOS		29	RABCD
13	TNEG		28	RMSYNC
14	INT		27	RFSYNC
15	SDI		26	RSER
16	SDO		25	RCHCLK
17	CS		24	RCLK
18	SCLK		23	RLCLK
19	SPS		22	RLINK
20	VSS		21	RYEL
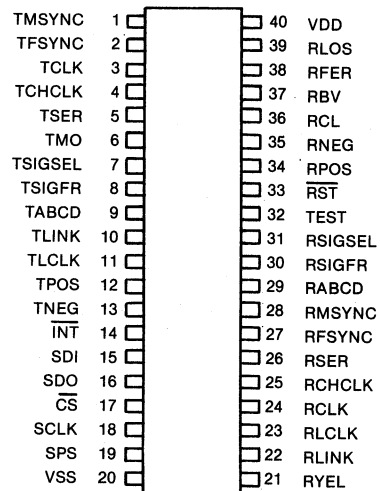
DESCRIPTION

The DS2180A is a monolithic CMOS device designed to implement primary rate (1.544 MHz) T-carrier transmission systems. The 193S framing mode is intended to support existing Ft/Fs applications (12 frames/superframe). The 193E framing mode supports the extended superframe format (24 frames/superframe). Clear channel capability is provided by selection of appropriate zero suppression and signaling modes.

Several functional blocks exist in the transceiver. The transmit framer/formatter generates appropriate framing bits, inserts robbed bit signaling, supervises zero suppression, generates alarms, and provides output clocks useful for data conditioning and decoding.

The receive synchronizer establishes frame and multiframe boundaries by identifying frame signaling bits, extracts signaling data, reports alarms and transmission errors, and provides output clocks useful for data conditioning and decoding.

The control block is shared between transmit and receive sides. This block determines the frame, zero suppression, alarm and signaling formats. User access to the control block is by one of two modes.

In the processor mode pins 14 through 18 are a microprocessor/microcontroller compatible serial port which can be used for device configuration, control and status monitoring.

In the hardware mode no offboard processor is required. Pins 14 through 18 are reconfigured into "hardwired" select pins. Features such as selective "clear" DS0 channels, insertion of idle code and alteration of sync algorithm are unavailable in the hardware mode.

DS2180A BLOCK DIAGRAM Figure 1

TMSYNC → Transmit Timing → TSIGSEL
TFSYNC → Transmit Timing → TMO
TCLK → Transmit Timing → TCHCLK
TLCLK ← Transmit Timing → TSIGFR

F-Bit Data

TLINK → Data Selector
TSER → Data Selector
TABCD → Data Selector

Yellow Alarm

Bipolar Coder → TPOS
Bipolar Coder → TNEG

CRC

⌐ VDD
= VSS

INT ← Serial Control Interface
CS → Serial Control Interface
SCLK → Serial Control Interface
SDI → Serial Control Interface
SDO ← Serial Control Interface
SPS → Serial Control Interface

Information Registers

← RST
← TEST

RYEL ← Yellow Alarm Detect

Code Gen

Receive Sync Controller → RLOS
Receive Sync Controller → RBV
Receive Sync Controller → RCL

RSER ← Data Demux
RABCD ← Data Demux
RLINK ← Data Demux

Bipolar Decoder ← RPOS
Bipolar Decoder ← RNEG

RCLK

RLCLK ← Receive Timing
RSIGFR ← Receive Timing
RSIGSEL ← Receive Timing
RCHCLK ← Receive Timing
RMSYNC ← Receive Timing
RFSYNC ← Receive Timing

Synchronizer

CRC

→ RFER

TRANSMIT PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	TMSYNC	I	**Transmit Multiframe Sync.** May be pulsed high at multiframe boundaries to reinforce multiframe alignment, or tied low, which allows internal multiframe counter to free run.
2	TFSYNC	I	**Transmit Frame Sync.** Rising edge identifies frame boundary; may be pulsed every frame to reinforce internal frame counter, or tied low (allowing TMSYNC to establish frame and multiframe alignment).
3	TCLK	I	**Transmit Clock.** 1.544 MHz primary clock.
4	TCHCLK	O	**Transmit Channel Clock.** 192 KHz clock which identifies time slot (channel) boundaries. Useful for parallel to serial conversion of channel data.
5	TSER	I	**Transmit Serial Data.** NRZ data input, sampled on falling edge of TCLK.
6	TMO	O	**Transmit Multiframe Out.** Output of internal multiframe counter, indicates multiframe boundaries. 50% duty cycle.
7	TSIGSEL	O	**Transmit Signaling Select.** .667 KHz clock which identifies signaling frames A and C in 193E framing. 1.33 KHz clock in 193S.
8	TSIGFR	O	**Transmit Signaling Frame.** High during signaling frames, low otherwise.
9	TABCD	I	**Transmit ABCD Signaling.** When enabled via TCR.4, sampled during channel LSB time in signaling frames on falling edge of TCLK.
10	TLINK	I	**Transmit Link Data.** Sampled during the F-bit time (falling edge of TCLK) of odd frames for insertion into the outgoing data stream (193E-FDL insertion). Sampled during the F-bit time of even frames for insertion into the outgoing data (193S-External S-Bit insertion).
11	TLCLK	O	**Transmit Link Clock.** 4 KHz demand clock for TLINK input.
12 13	TPOS TNEG	O	**Transmit Bipolar Data Outputs.** Updated on rising edge of TCLK.

PORT PIN DESCRIPTION Table 2

PIN	SYMBOL	TYPE	DESCRIPTION
14	$\overline{\text{INT}}$[1]	O	**Receive Alarm Interrupt.** Flags host controller during alarm conditions. Active low, open drain output.
15	SDI[1]	I	**Serial Data In.** Data for on-board registers. Sampled on rising edge of SCLK.
16	SDO[1]	O	**Serial Data Out.** Control and status information from on-board registers. Updated on falling edge of SCLK, tri-stated during serial port write or when $\overline{\text{CS}}$ is high.
17	$\overline{\text{CS}}$[1]	I	**Chip Select.** Must be low to write or read the serial port.
18	SCLK[1]	I	**Serial Data Clock.** Used to write or read the serial port registers.
19	SPS	I	**Serial Port Select.** Tie to VDD to select serial port. Tie to VSS to select hardware mode.

NOTES: 1. Multifunction pins, see hardware mode description.

5

POWER AND TEST PIN DESCRIPTION Table 3

PIN	SYMBOL	TYPE	DESCRIPTION
20	VSS	-	**Signal Ground.** 0.0 volts.
32	TEST	I	**Test Mode.** Tie to VSS for normal operation.
40	VDD	-	**Positive Supply.** 5.0 volts.

RECEIVE PIN DESCRIPTION Table 4

PIN	SYMBOL	TYPE	DESCRIPTION
21	RYEL	O	**Receive Yellow Alarm.** Transitions high when yellow alarm detected, goes low when alarm clears.
22	RLINK	O	**Receive Link Data.** Updated with extracted FDL data one RCLK before start of odd frames (193E) and held until next update. Updated with extracted S-bit data one RCLK before start of even frames (193S) and held until next update.
23	RLCLK	O	**Receive Link Clock.** 4 KHz demand clock for RLINK.
24	RCLK	I	**Receive Clock.** 1.544 MHz primary clock.
25	RCHCLK	O	**Receive Channel Clock.** 192 KHz clock, identifies time slot (channel) boundaries.
26	RSER	O	**Receive Serial Data.** Received NRZ serial data, updated on rising edges of RCLK.
27	RFSYNC	O	**Receive Frame Sync.** Extracted 8 KHz clock, one RCLK wide, indicates F-Bit position in each frame.
28	RMSYNC	O	**Receive Multiframe Sync.** Extracted multiframe sync; edge indicates start of multiframe, 50% duty cycle.
29	RABCD	O	**Receive ABCD Signaling.** Extracted signaling data output, valid for each channel time in signaling frames. In non-signaling frames, RABCD outputs the LSB of each channel word.
30	RSIGFR	O	**Receive Signaling Frame.** High during signaling frames, low during resync and non-signaling frames.
31	RSIGSEL	O	**Receive Signaling Select.** In 193E framing a .667 KHz clock which identifies signaling frames A and C. A 1.33 KHz clock in 193S.
33	$\overline{\text{RST}}$	I	**Reset.** A high-low transition clears all internal registers and resets receive side counters. A high-low-high transition will initiate a receive resync.
34	RPOS	I	**Receive Bipolar Data Inputs.** Sampled on falling edge of RCLK. Tie together to receive NRZ data and disable bipolar violation monitoring circuitry.
35	RNEG		
36	RCL	O	**Receive Carrier Loss.** High if 32 consecutive "0's" appear at RPOS and RNEG, goes low after next "1."
37	RBV	O	**Receive Bipolar Violation.** High during accused bit time at RSER if bipolar violation detected, low otherwise.

38	**RFER**	O	**Receive Frame Error.** High during F-Bit time when F_T or F_S errors occur (193S), or when FPS or CRC errors occur (193E). Low during resync.
39	**RLOS**	O	**Receive Loss of Sync.** Indicates sync status; high when internal resync is in progress, low otherwise.

REGISTER SUMMARY Table 5

REGISTER	ADDRESS	T/R[1]	DESCRIPTION/FUNCTION
RSR	0000	R[2]	**Receive Status Register.** Reports all receive alarm conditions.
RIMR	0001	R	**Receive Interrupt Mask Register.** Allows masking of individual alarm generated interrupts.
BVCR	0010	R	**Bipolar Violation Count Register.** 8 bit presettable counter which records individual bipolar violations.
ECR	0011	R	**Error Count Register.** 2 independent 4-bit counters which record OOF occurrences, and individual frame bit or CRC errors.
CCR[3]	0100	T/R	**Common Control Register.** Selects device operating characteristics common to receive and transmit sides.
RCR[3]	0101	R	**Receive Control Register.** Programs device operating characteristics unique to the receive side.
TCR[3]	0110	T	**Transmit Control Register.** Selects additional transmit side modes.
TIR1 **TIR2** **TIR3**	0111 1000 1001	T T T	**Transmit Idle Registers.** Designate which outgoing channels are to be substituted with idle code.
TTR1 **TTR2** **TTR3**	1010 1011 1100	T T T	**Transmit Transparent Registers.** Designate which outgoing channels are to be treated transparently. (No robbed bit signaling or bit 7 zero insertion.)
RMR1 **RMR2** **RMR3**	1101 1110 1111	R R R	**Receive Mark Registers.** Designate which incoming channels are to be replaced with idle or digital milliwatt codes (under control of RCR).

NOTES: 1. Transmit or receive side register.
      2. RSR is a read only register, all other registers are read/write.
      3. Reserved bit locations in the control registers should be programmed to 0, to maintain compatibility with future transceiver products.

SERIAL PORT INTERFACE
Pins 14 through 18 of the DS2180A serve as a microprocessor/microcontroller compatible serial port. Sixteen on-board registers allow the user to update operational characteristics and monitor device status via a host controller, minimizing hardware interfaces. Port read/write timing is unrelated to the system transmit and receive timing, allowing asynchronous reads and/or writes by the host.

ADDRESS/COMMAND
Reading or writing the control, configuration or status registers requires writing one address/command byte prior to transferring register data. The first bit written (LSB) of the address/command word specifies register read or write. The following 4 bit nibble identifies register address. The next two bits are reserved and must be set to zero for proper operation. The last bit of the address/command word enables burst mode when set; the burst mode causes all registers to be consecutively written or read. *Data is written to and read from the transceiver LSB first.*

CHIP SELECT AND CLOCK CONTROL
All data transfers are initiated by driving the $\overline{CS}$ input low. Input data is latched on the rising edge of SCLK and *must be valid during the previous low period of SCLK to prevent momentary corruption of register data during writes.* Data is output on the falling edge of SCLK and held to the next falling edge. All data transfers are terminated if the $\overline{CS}$ input transitions high. Port control logic is disabled and SDO is tristated when $\overline{CS}$ is high.

DATA I/O
Following the 8 SCLK cycles that input an address/command byte to write, a data byte is strobed into the addressed register on the rising edges of the next 8 SCLK cycles. Following an address/command word to read, contents of the selected register are output on the falling edges of the next 8 SCLK cycles. The SDO pin is tristated during device write, and may be tied to SDI in applications where the host processor has a bidirectional I/O pin.

BURST MODE
The burst mode allows all on-board registers to be consecutively read or written by the host processor. A burst read is used to poll all registers; RSR contents will be unaffected. This feature minimizes device initialization time on power-up or system reset. Burst mode is initiated when ACB.7 is set and the address nibble is 0000. Burst is terminated by low-high transition on $\overline{CS}$.

ACB: ADDRESS COMMAND BYTE Figure 2

(MSB)   (LSB)

BM	—	—	ADD3	ADD2	ADD1	ADD0	R/W̄
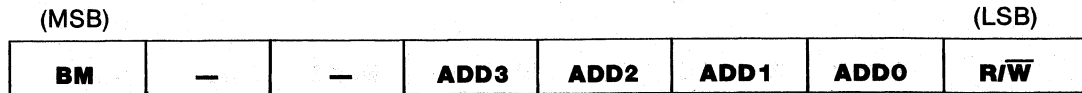
SYMBOL	POSITION	NAME AND DESCRIPTION
BM	ACB.7	**Burst Mode.** If set (and ACB.1 through ACB.4 = 0) burst read or write is enabled
—	ACB.6	Reserved, must be 0 for proper operation
—	ACB.5	Reserved, must be 0 for proper operation
ADD3	ACB.4	MSB of register address
ADD0	ACB.1	LSB of Register address
R/W̄	ACB.0	**Read/Write Select.** 0 = write addressed register 1 = read addressed register

SERIAL PORT READ/WRITE Figure 3

CS̄

SCLK

SDI, SDO^{1,2} — R/W̄ ╳ ADD0 ╳ ADD1 ╳ ADD2 ╳ ADD3 ╳ 0 ╳ 0 ╳ BM ╳ D0 ╳ D1 ╳ D2 ╳ D3 ╳ D4 ╳ D5 ╳ D6 ╳ D7 —

— ADDRESS/COMMAND — / — DATA INPUT/OUTPUT —
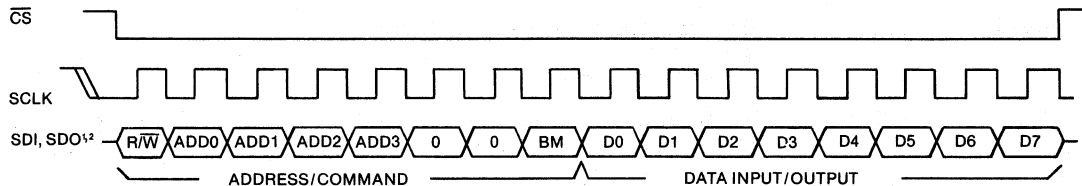
NOTES: 1. SDI sampled on rising edge of SCLK
2. SDO updated on falling edge of SCLK

COMMON CONTROL REGISTER Figure 4

(MSB)   (LSB)

—	FRSR2	EYELMD	FM	SYELMD	B8ZS	B7	LPBK

SYMBOL	POSITION	NAME AND DESCRIPTION
—	CCR.7	Reserved, must be 0 for proper operation
FRSR2	CCR.6	**Function of Rec Status Register 2.** 0 = Detected B8ZS code words reported at RSR.2 1 = COFA (Change-of-Frame Alignment) reported at RSR.2 when last resync resulted in change of frame or multiframe alignment.
EYELMD	CCR.5	**193E Yellow Mode Select.** 0 = Yellow alarm is a repeating pattern set of 00 hex and FF hex 1 = Yellow alarm is a "0" in the bit 2 position of all channels
FM	CCR.4	**Frame Mode Select.** 0 = D4 (193S, 12 frames/superframe) 1 = Extended (193E, 24 frames/superframe)
SYELMD	CCR.3	**193S Yellow Mode Select.** Determines yellow alarm type to be transmitted and detected while in 193S framing. If set, yellow alarms are a "1" in the S-bit position of frame 12; if cleared, yellow alarm is a "0" in bit 2 of all channels. Does not affect 193E yellow alarm operation.
B8ZS	CCR.2	**Bipolar eight zero substitution.** 0 = No B8ZS 1 = B8ZS Enabled
B7	CCR.1	**Bit seven zero suppression.** If CCR.1 = 1, channels with an all zero content will be transmitted with bit 7 forced to "1." If CCR.1 = 0, no bit 7 stuffing occurs.
LPBK	CCR.0	**Loopback.** When set, the device internally loops output transmit data into the incoming receive data buffers and TCLK is internally substituted for RCLK.

LOOPBACK (Refer to Figure 4)

Enabling loopback will typically induce an out-of-frame "OOF" condition. If appropriate bits are set in the receive control register, the receiver will resync to the looped transmit frame alignment. During the looped condition, the transmit outputs (TPOS, TNEG) will transmit unframed all "1's." All operating modes (B8ZS, alarm, signaling, etc.) except for blue alarm transmission are available in loopback.

BIT SEVEN STUFFING

Existing systems meet "ones" density requirements by forcing bit 7 of all zero channels to 1. Bit 7 stuffing is "globally" enabled by asserting bit CCR.1, and may be disabled on an individual channel basis by setting appropriate bits in TTR1-TTR3.

B8ZS

The DS2180A supports existing and emerging zero suppression formats. Selection of B8ZS coding maintains system "ones" density requirements without disturbing data integrity as required in emerging clear channel applications. B8ZS coding replaces 8 consecutive outgoing zeros with a B8ZS code word. Any received B8ZS code word is replaced with all zeros.

TCR: TRANSMIT CONTROL REGISTER Figure 5

(MSB)   (LSB)

OOF	TFPT	TCP	RBSE	TIS	193SI	TBL	TYEL

SYMBOL	POSITION	NAME AND DESCRIPTION
ODF	TCR.7	**Output Data Format.** 0 = Bipolar data at TPOS and TNEG. 1 = NRZ data at TPOS; TNEG = 0
TFPT	TCR.6	**Transmit Framing Pass-through.** 0 = FT/FPS sourced internally. 1 = FT/FPS sampled at TSER during F-bit time
TCP	TCR.5	**Transmit CRC Pass-through.** 0 = Transmit CRC code internally generated. 1 = TSER sampled at CRC F-bit time for external CRC insertion.
RBSE	TCR.4	**Robbed Bit Signaling Enable.** 1 = signaling inserted in all channels during signaling frames. 0 = no signaling inserted. (The TTR registers allow the user to disable signaling insertion on selected DS0 channels.)
TIS	TCR.3	**Transmit Idle Code Select.** Determines idle code format to be inserted into channels marked by the TIR registers. 0 = insert 7F (Hex) into marked channels. 1 = insert FF (Hex) into marked channels.
193SI	TCR.2	**193S S-bit Insertion.** Determines source of transmitted S-bit. 0 = internal S-bit generator. 1 = external (sampled at TLINK input)
TBL	TCR.1	**Transmit Blue Alarm.** 0 = disabled. 1 = enabled
TYEL	TCR.0	**Transmit Yellow Alarm.** 0 = disabled. 1 = enabled

TRANSMIT BLUE ALARM (Refer to Figure 5)
The blue alarm (also known as the AIS, Alarm Indication Signal) is an unframed, all 1's sequence enabled by asserting TCR.1. Blue alarm overrides all other transmit data patterns and is disabled by clearing TCR.1. Use of the TIR registers allows a framed, all 1's alarm transmission if required by the network.

TRANSMIT YELLOW ALARM
In 193E framing a yellow alarm is a repeating pattern set of FF (Hex) and 00 (Hex) on the 4 KHz facility data link (FDL). In 193S framing, the yellow alarm format is dependent on the state of bit CCR.3. In all modes, yellow alarm is enabled by asserting TCR.0 and disabled by clearing TCR.0.

TRANSMIT SIGNALING
When enabled (via TCR.4) channel signaling is inserted in frames 6 and 12, (193S) or 6, 12 and 18 and 24 (193E) in the 8th bit position of every channel word. Signaling data is sampled at TABCD on the falling edge of TCLK during bit 8 of each input word during signaling frames. Logical combination of clocks TMO, TSIGFR and TSIGSEL allow external multiplexing of separate serial links for A, B or A, B, C, D signaling sources.

TTR1-TTR3: TRANSMIT TRANSPARENCY REGISTERS Figure 6

(MSB)   (LSB)

CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TTR1
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TTR2
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TTR3

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	TTR3.7	**Transmit Transparent Registers.** Each of these bit positions represents a DS0 channel in the outgoing frame. When
CH1	TTR1.0	set the corresponding channel is transparent.

TIR1-TIR3: TRANSMIT IDLE REGISTERS Figure 7

(MSB)   (LSB)

CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TIR1
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TIR2
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TIR3

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	TIR3.7	**Transmit Idle Registers.** Each of these bit positions represents a DS0 channel in the outgoing frame. When set,
CH1	TIR1.0	the corresponding channel will output an idle code format determined by TCR.3.

TRANSMIT CHANNEL TRANSPARENCY

Individual DS0 channels in the T1 frame may be programmed clear (no inserted robbed bit signaling and no bit 7 zero suppression) by setting the appropriate bits in the transmit transparency registers. Channel transparency is required in mixed voice/data or data-only environments such as ISDN, where data integrity must be maintained.

TRANSMIT IDLE CODE INSERTION

Individual outgoing channels in the frame can be programmed with idle code by asserting the appropriate bits in the transmit idle registers. One of two idle code formats, 7F (Hex) and FF (Hex) may be selected by the user via TCR.3. If enabled, robbed bit signaling data is inserted into the idle channel, unless the appropriate TTR bit is set for that channel. This feature eliminates external hardware currently required to intercept and stuff unoccupied channels in the DS1 bit stream.

TSER   TLINK   TABCD

```
                    ┌─────────┐
                    │  F BIT  │
                    └─────────┘
                       TSER

                    ┌─────────┐    Y
                    │  IDLE   │────────────┐
                    └─────────┘            │
                       │ N                 │
                      TSER               IDLE
                                           │
        Y          ┌─────────┐           ┌─────────┐  Y
   ────────────────│  CLEAR  │           │  CLEAR  │──────────┐
                   └─────────┘           └─────────┘          │
                      │ N                   │ N               │
                     TSER                 IDLE              IDLE
                                 ●
   TSER      Y    ┌─────────┐         ┌─────────┐  Y
          ───────│   SIG   │          │   SIG   │────────┐
                 └─────────┘          └─────────┘        │
   TSER + ABCD      │ N                  │ N             │
                   TSER               IDLE          IDLE + ABCD
         Y  ┌──────────┐    Y  ┌──────────┐
        ────│ B7 STUFF │    ───│ B7 STUFF │
            └──────────┘       └──────────┘
                │ N                 │ N
 TSER + ABCD  TSER + ABCD   TSER + B7   TSER
    + B7
```

```
┌──────────────────────────────────────────────────────────────┐
│            193S YELLOW ALARM — B2 STUFF                         │
└──────────────────────────────────────────────────────────────┘
                          │
┌──────────────────────────────────────────────────────────────┐
│                         B8ZS                                   │
└──────────────────────────────────────────────────────────────┘
                          │
┌──────────────────────────────────────────────────────────────┐
│                     BLUE or LPBK                               │
└──────────────────────────────────────────────────────────────┘
                          │
                     TPOS, TNEG
```

5

193S TRANSMIT MULTIFRAME TIMING Figure 9

NOTES: 1. Transmit frame and multiframe timing may be established in one of four ways:
   a) With TFSYNC tied low, TMSYNC may be pulsed high once every multi-frame period to establish multiframe boundaries, allowing internal counters to determine frame timing.
   b) TFSYNC may be pulsed every 125 microseconds; pulsing TMSYNC once establishes multiframe boundaries.
   c) TMSYNC and TFSYNC may be continuously pulsed to establish and rein-force frame and superframe timing.
   d) If TMSYNC is tied low and TFSYNC is pulsed at frame boundaries, the transmitter will establish an arbitrary multiframe boundary as indicated by TMO.
2. Channels in which robbed bit signaling is enabled will sample TABCD during the LSB bit time in frames indicated.
3. When external S-bit insertion is enabled, TLINK will be sampled during the F-bit time of even frames and inserted into the outgoing data stream.

193E TRANSMIT MULTIFRAME TIMING Figure 10

FRAME # 24| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |10|11|12|13|14|15|16|17|18|19|20|21|22|23|24| 1

TFSYNC[1]

TMSYNC[1]

TMO[1]

TSIGSEL

TSIGFR

TLCLK

TABCD[2]

TLINK[3]

5

NOTES: 1. Transmit frame and multiframe timing may be established in one of four ways:
   a) With TFSYNC tied low, TMSYNC may be pulsed high once every multi-frame period to establish multiframe boundaries, allowing internal counters to determine frame timing.
   b) TFSYNC may be pulsed every 125 microseconds; pulsing TMSYNC once establishes multiframe boundaries.
   c) TMSYNC and TFSYNC may be continuously pulsed to establish and rein-force frame and superframe timing.
   d) If TMSYNC is tied low and TFSYNC is pulsed at frame boundaries, the transmitter will establish an arbitrary multiframe boundary as indicated by TMO.

2. Channels in which robbed bit signaling is enabled will sample TABCD during the LSB bit time in frames indicated.

3. TLINK is sampled during the F-bit time of odd frames and inserted into the out-going data stream (FDL data).

TRANSMIT MULTIFRAME BOUNDARY TIMING Figure 11
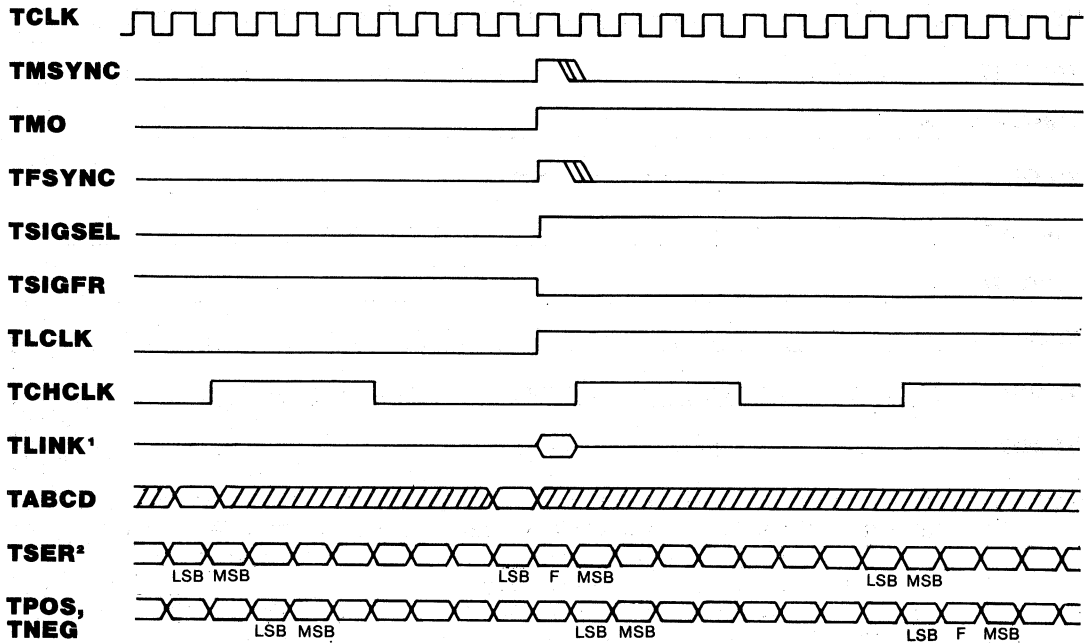
NOTES: 1. TLINK timing shown is for 193E framing; in 193E framing, TLINK is sampled as indicated for insertion into F-bit position of odd frames. When S-bit insertion is enabled in 193S, TLINK is sampled during even frames.

2. If TCR.5 = 1; TSER is sampled during the F-bit time of CRC frames for insertion into the outgoing data stream (193E Framing only).

RECEIVE CONTROL REGISTER Figure 12

(MSB)   (LSB)

ARC	OOF	RCI	RCS	SYNCC	SYNCT	SYNCE	RESYNC

SYMBOL	POSITION	NAME AND DESCRIPTION
ARC	RCR.7	**Auto Resync Criteria.** 0 = Resync on OOF or RCL event. 1 = Resync on OOF only.
OOF	RCR.6	**Out-of-frame (OOF) Condition Detection.** 0 = 2 of 4 framing bits in error 1 = 2 of 5 framing bits in error
RCI	RCR.5	**Receive Code Insert.** When set, the receive code selected by RCR.4 is inserted into channels marked by RMR registers. If clear, no code is inserted.
RCS	RCR.4	**Receive Code Select.** 0 = idle code (7F Hex) 1 = digital milliwatt
SYNCC	RCR.3	**Sync Criteria.** Determines the type of algorithm utilized by the receive synchronizer and differs for each frame mode. **193S Framing (CCR.4 = 0).** 0 = synchronize to frame boundaries using F_T pattern, then search for multiframe by using F_S. 1 = cross couple F_T and F_S patterns in sync algorithm. **193E Framing (CCR.4 = 1).** 0 = normal sync (utilizes FPS only) 1 = validate new alignment with CRC before declaring sync.
SYNCT	RCR.2	**Sync Time.** If set, 24 consecutive F-bits of the framing pattern must be qualified before sync is declared. If clear, 10 bits are qualified.
SYNCE	RCR.1	**Sync Enable.** If clear, the transceiver will automatically begin a resync if 2 of the previous 4 or 5 framing bits were in error, or if carrier loss is detected. If set, no auto resync occurs.
RESYNC	RCR.0	**Resync.** When toggled low to high, the transceiver will initiate resync immediately. The bit must be cleared, then set again for subsequent resyncs.

5

RECEIVE CODE INSERTION

Incoming receive channels can be replaced with idle (7F Hex) or digital milliwatt (u-LAW format) codes. The receive mark registers indicate which channels are inserted. When set, bit RCR.5 serves as a "global" enable for marked channels, and bit RCR.4 selects inserted code format: 0 = idle code, 1 = digital milliwatt.

RECEIVE SYNCHRONIZER

Bits RCR.0 through RCR.3 allow the user to control operational characteristics of the synchronizer. Sync algorithm, candidate qualify testing, auto resync, and command resync modes may be altered at any time in response to changing span conditions.

RECEIVE SIGNALING

Robbed bit signaling data is presented at RABCD during each channel time in signaling frames for all 24 incoming channels. Logical combination of clocks RMSYNC, RSIGFR and RSIGSEL allow the user to identify and extract AB or ABCD signaling data.

RMR1-RMR3: RECEIVE MARK REGISTERS Figure 13

(MSB)   (LSB)

CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RMR1
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RMR2
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RMR3

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	RMR3.7	**Receive Mark Registers.** Each of these bit positions represents a DS0 channel in the incoming T1 frame. When set the corresponding channel will output codes determined by RCR.4 and RCR.5.
CH1	RMR1.0	

193S RECEIVE MULTIFRAME TIMING Figure 14

FRAME # 12| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10| 11 | 12| 1 | 2 | 3 | 4 | 5 | 6

RFSYNC

RMSYNC

RSIGSEL

RSIGFR

RLCLK
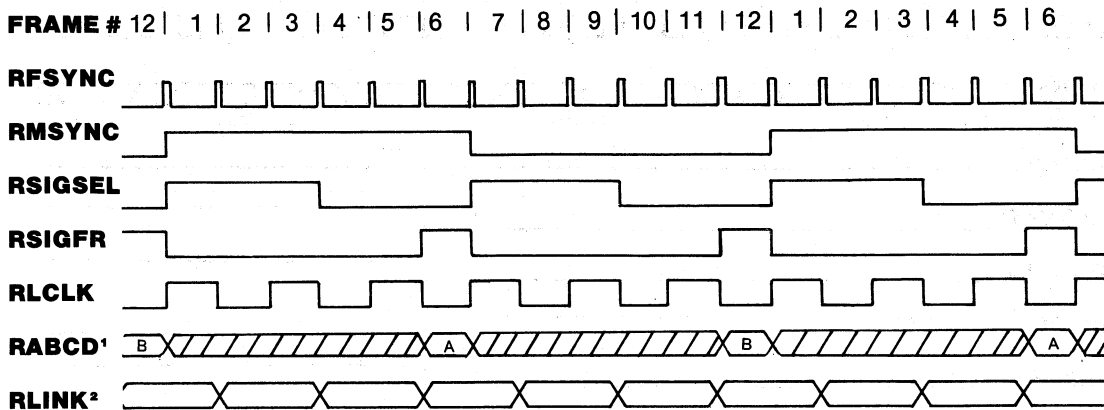
RABCD[1]

RLINK[2]

NOTES: 1. Signaling data is updated during signaling frames on channel boundaries. RABCD is the LSB of each channel word in non-signaling frames.
2. RLINK data (S-bit) is updated one bit time prior to S-bit frames and held for two frames.

193E RECEIVE MULTIFRAME TIMING Figure 15

FRAME # 24| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10| 11| 12| 13| 14| 15| 16 | 17| 18| 19| 20| 21| 22| 23| 24|

RFSYNC

RMSYNC

RSIGSEL

RSIGFR

RLCLK
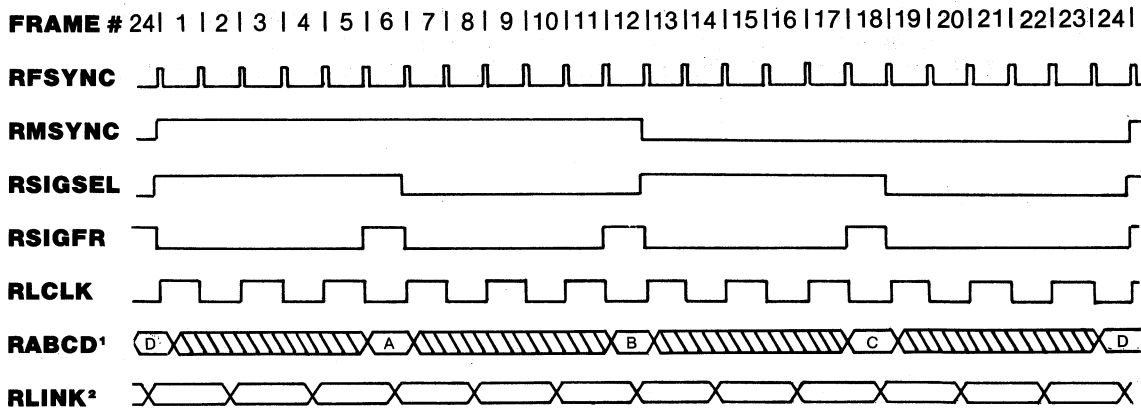
RABCD[1]

RLINK[2]

NOTES: 1. Signaling data is updated during signaling frames on channel boundaries. RABCD outputs the LSB of each channel word in non-signaling frames.
2. RLINK data (FDL-bit) is updated one bit time prior to odd frames and held for two frames.

5

RECEIVE MULTIFRAME BOUNDARY TIMING Figure 16
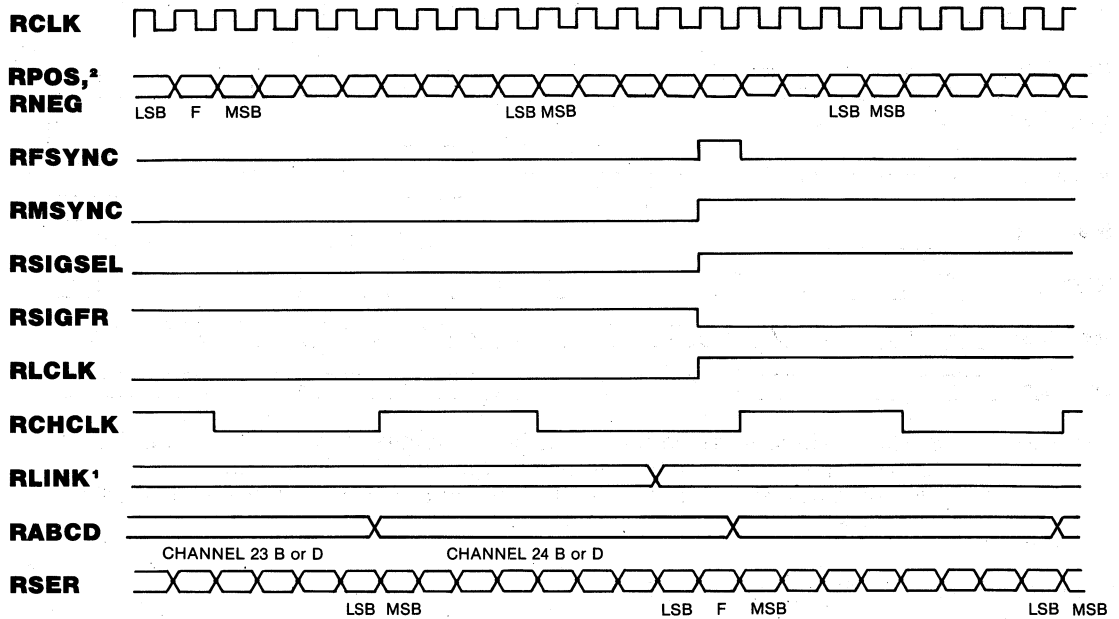
NOTES: 1. RLINK timing is shown for 193E; in 193S RLINK is updated on even frame boundaries and is held across multiframe edges.

2. Total delay from RPOS and RNEG to RSER output is 13 RCLK periods.

RSR: RECEIVE STATUS REGISTER Figure 17

(MSB)   (LSB)

BVCS	ECS	RYEL	RCL	FERR	B8ZSD	RBL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
BVCS	RSR.7	**Bipolar Violation Count Saturation.** Set when the 8-bit counter at BVCR saturates.
ECS	RSR.6	**Error Count Saturation.** Set when either of the 4-bit counters at ECR saturates.
RYEL	RSR.5	**Receive Yellow Alarm.** Set when yellow alarm detected. (Detected yellow alarm format determined by CCR.4 and CCR.3.)
RCL	RSR.4	**Receive Carrier Loss.** Set when 32 consecutive "0's" appear at RPOS and RNEG.
FERR	RSR.3	**Frame Bit Error.** Set when F_T (193S) or FPS (193E) bit error occurs.
B8ZSD	RSR.2	**Bipolar Eight Zero Substitution Detect.** Set when B8ZS code word detected.
RBL	RSR.1	**Receive Blue Alarm.** Set when 2 consecutive frames have less than 3 zeros (total) in the data stream (F-bit positions not tested).
RLOS	RSR.0	**Receive Loss of Sync.** Set when resync is in process; if RCR.1 = 0, RLOS transitions high on an OOF event or carrier loss, indicating auto resync.

5

RECEIVE ALARM REPORTING
Incoming serial data is monitored by the transceiver for alarm occurrences. Alarm conditions are reported in two ways: via transitions on the alarm output pins and registered interrupt, in which the host controller reads the RSR in response to an alarm driven interrupt. Interrupts may be direct, in which the transceiver demands service for a real time alarm, or count-overflow triggered, in which an on-board alarm event counter exceeds a user-programmed threshold. The user may mask individual alarm conditions by clearing the appropriate bits in the receive interrupt mask register (RIMR).

ALARM SERVICING
The host controller must service the transceiver in order to clear an interrupt condition. Clearing appropriate bits in the RIMR will unconditionally clear an interrupt. Direct interrupts (those driven from real-time alarms) will be cleared when the RSR is directly read, unless the alarm condition still exists. Count-overflow interrupts (BVCS, FCS) are not cleared by a direct read of the RSR. They will be cleared only when the user presets the appropriate count register to a value other than all "1s." A burst read of the RSR will not clear an interrupt condition.

RIMR: RECEIVE INTERRUPT MASK REGISTER Figure 18

(MSB)   (LSB)

BVCS	ECS	RYEL	RCL	FERR	B8ZSD	RBL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
BVCS	RIMR.7	**Bipolar Violation Count Saturation Mask.** 1 = interrupt enabled 0 = interrupt masked
ECS	RIMR.6	**Error Count Saturation Mask.** 1 = interrupt enabled 0 = interrupt masked
RYEL	RIMR.5	**Receive Yellow Alarm Mask.** 1 = interrupt enabled 0 = interrupt masked
RCL	RIMR.4	**Receive Carrier Loss Mask.** 1 = interrupt enabled 0 = interrupt masked
FERR	RIMR.3	**Frame Bit Error Mask.** 1 = interrupt enabled 0 = interrupt masked
B8ZSD	RIMR.2	**B8ZS Detect Mask.** 1 = interrupt enabled 0 = interrupt masked
RBL	RIMR.1	**Receive Blue Alarm Mask.** 1 = interrupt enabled 0 = interrupt masked
RLOS	RIMR.0	**Receive Loss of Sync Mask.** 1 = interrupt enabled 0 = interrupt masked

ALARM COUNTERS

The three on-board alarm event counters allow the transceiver to monitor and record error events without processor intervention on each event occurrence. All of these counters are presettable by the user, establishing an event count interrupt threshold. As each counter saturates, the next error event occurrence will set a bit in the RSR and generate an interrupt unless masked. The user may read these registers at any time; in many systems, the host will periodically poll these registers to establish link error rate performance.

OOF EVENTS AND ERRORED SUPERFRAMES

Out of frame is declared when at least two of four (or five) consecutive framing bits are in error. F_T bits are tested for OOF occurrence in 193S, the FPS bits are tested in 193E. OOF events are recorded by the 4-bit OOF counter in the error count register. In the 193E framing mode, the OOF event is logically "OR'ed" with an on-chip generated CRC checksum. This event, known as errored superframe, is recorded by the 4-bit ESF error counter in the error count register. In the 193S framing mode, the 4-bit ESF error counter records individual F_T and F_S errors when RCR.3 = 1, or F_T errors only when RCR.3 = 0.

BVCR: BIPOLAR VIOLATION COUNT REGISTER Figure 19

(MSB)   (LSB)

BVD7	BVD6	BVD5	BVD4	BVD3	BVD2	BVD1	BVD0

SYMBOL	POSITION	NAME AND DESCRIPTION
BVD7	BVCR.7	MSB of bipolar violation count
BVD0	BVCR.0	LSB of bipolar violation count

This 8 bit binary up counter saturates at 255 and will generate an interrupt for each occurrence of a bipolar violation once saturated (RIMR.7 = 1). Presetting this register allows the user to establish specific count interrupt thresholds. The counter will count "up" to saturation from the preset value, and may be read at any time. Counter increments occur at all times and are not disabled by resync.

ECR: ERROR COUNT REGISTER Figure 20

(MSB)   (LSB)

OOFD3	OOFD2	OOFD1	OOFD0	ESFD3	ESFD2	ESFD1	ESFD0

|←——————— OOF COUNT ———————→|←——————— ESF ERROR COUNT ———————→|

SYMBOL	POSITION	NAME AND DESCRIPTION
OOFD3	ECR.7	MSB of OOF event count
OOFD0	ECR.4	LSB of OOF event count
ESFD3	ECR.3	MSB of extended superframe error count
ESFD0	ECR.0	LSB of extended superframe error count

These separate 4-bit binary up counters saturate at a count of 15 and will generate an interrupt for each occurrence of an OOF event or an ESF error event after saturation (RIMR.6 = 1). Presetting these counters allows the user to establish specific count interrupt thresholds. The counters will count "up" to saturation from the preset value, and may be read at any time. These counters share the same register address, and must be written to or read from simultaneously.

The OOF counter records out-of-frame events in both 193S and 193E. The ESF error counter records errored superframes in 193E. In 193S the ESF counter records individual F_T and F_S errors when RCR.3 = 1; F_T errors only when RCR.3 = 0. ECR counter increments are disabled when resync is in progress (RLOS high).

5

ALARM OUTPUTS

The transceiver also provides direct alarm outputs for applications when additional decoding and demuxing are required to supplement the on-board alarm logic.

RLOS OUTPUT

The receive loss of sync output indicates the status of the receiver synchronizer circuitry: when high, an off-line resynchronization is in progress and a high-low transition indicates resync is complete. The RLOS bit (RSR.0) is a "latched" version of the RLOS output. If the auto-resync mode is selected (RCR.1 = 0) RLOS is a real time indication of a carrier loss or OOF event occurrence.

RYEL OUTPUT

The yellow alarm output transitions high when a yellow alarm is detected. A high-low transition indicates the alarm condition has been cleared. The RYEL bit (RSR.5) is a "latched" version of the RYEL output. In 193E framing, the yellow alarm pattern detected is 16 pattern sets of 00 (Hex) and FF (Hex) received at RLINK. In 193S framing the yellow alarm format is dependent on CCR.3: if CCR.3 = 0, the RYEL output transitions high if bit 2 of 256 or more consecutive channels is 0; if CCR.3 = 1, yellow alarm is declared when the S-bit received in frame 12 is 1.

RBV OUTPUT

The bipolar violation output transitions high when accused bit emerges at RSER. RBV will go low at the next bit time if no additional violations are detected.

RFER OUTPUT

The receive frame error output transitions high at the F-bit time and is held high for two bit periods when a frame bit error occurs. In 193S framing F_T and F_S patterns are tested. The FPS pattern is tested in 193E framing. Additionally, in 193E framing, RFER reports a CRC error by a low-high-low transition (one bit period wide) one half RCLK period before a low-high transition on RMSYNC.

RESET

A high-low transition on $\overline{RST}$ clears all registers and forces immediate receive resync when $\overline{RST}$ returns high. This reset has no effect on transmit frame, multiframe, or channel counters. $\overline{RST}$ must be held low on system power-up to insure proper initialization of transceiver counters and registers. Following reset, the host processor should restore all control modes by writing appropriate registers with control data.

ALARM OUTPUT TIMING Figure 21
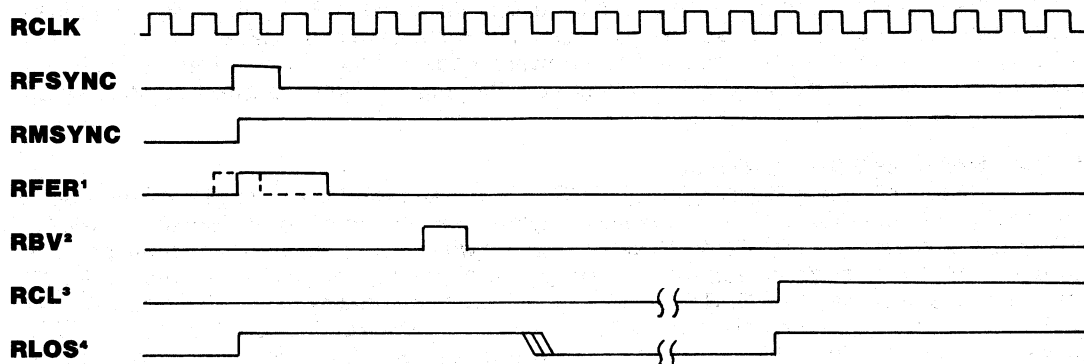
NOTES:
1. RFER transitions high during F-bit time if received framing pattern bit is in error. (Frame 12 F-bits in 193S are ignored if CCR.3 = 1.) Also, in 193E, RFER transitions ½ bit time before the rising edge of RMSYNC to indicate a CRC error for the previous multi-frame.
2. RBV indicates received bipolar violation and transitions high when accused bit emerges from RSER. If B8ZS is enabled, RBV will not report the zero replacement code.
3. RCL transitions high (during 32nd bit time) when 32 consecutive bits received are "0"; RCL transitions low when the next "1" is received.
4. RLOS transitions high during the F-bit time that caused an OOF event (any 2 of 4 consecutive F_T or FPS bits are in error) if auto-resync mode is selected (RCR.1 = 0). Resync will also occur when loss of carrier is detected (RCL = 1). When RCR.1 = 1, RLOS remains low until resync occurs, regardless of OOF or carrier loss flags. In this situation, resync is initiated only when RCR.0 transitions low-to-high or the RST pin transitions high-low-high.

5

HARDWARE MODE

For preliminary system prototyping or applications which do not require the features offered by the serial port, the transceiver can be reconfigured by the SPS pin. Tying SPS to VSS disables the serial port, clears all internal registers except CCR and TCR and redefines pins 14 through 18 as mode control inputs. The hardware mode allows device retrofit into existing applications where mode control and alarm conditioning hardware is often designed with discrete logic.

HARDWARE COMMON CONTROL

In the hardware mode bits TCR.2, CCR.4, TCR.0, CCR.1 and CCR.2 map to pins 14 through 18. The loopback feature (bit CCR.0) is enabled by tying pins 17 (zero suppression) and 18 (B8ZS) to 1. (The last states of pins 17 and 18 are latched as when both pins are taken high, preserving the current zero suppression mode). Robbed bit signalling (bit TCR.4) is enabled for all channels. The user may tie TSER to TABCD externally to disable signaling if so desired. Bit CCR.3 is forced to 0, which selects bit 2 yellow alarm in 193S framing. Contents of the RCR, as well as the remaining bit locations in the CCR and TCR, are cleared in the hardware mode. The RST input may be used to force immediate receiver resync, and has no effect on transmit.

HARDWARE MODE Table 6

PIN NUMBER	REGISTER BIT LOCATION	NAME AND DESCRIPTION
14	TCR-D2	**193S - S-bit insertion[3].** 1 = external; 0 = internal
15	CCR-D4	**Framing Mode Select.** 1 = 193E; 0 = 193S
16	TCR-D0	**Transmit Yellow Alarm[2][3].** 1 = enabled; 0 = disabled
17	CCR-D1	**Zero Suppression[1].** 1 = bit 7 stuffing 0 = transparent
18	CCR-D2	**B8ZS[1].** 1 = enabled; 0 = disabled

NOTES: 1. Tying pins 17 and 18 high enables loopback in the hardware mode.
2. Bit 2 (193S) and data link (193E) yellow alarms are supported.
3. S-bit yellow alarm (193S) is not internally supported; however, the user may elect to insert external S-bits for alarm purposes.

T1 Overview

FRAMING STANDARDS

The DS2180A is compatible with the existing Bell System D4 framing standard described in ATT PUB 43801 and the new extended superframe format (ESF) as described in ATT C.B. #142. In this document, D4 framing is referred to as 193S, and ESF (also known as Fe) is referred to as 193E. Programmable features of the DS2180A allow support of other framing standards which are derivatives of 193E and 193S. The salient differences between the 193S and 193E formats are the number of frames per superframe and use of the F-bit position. In 193S, 12 frames make up a superframe; in 193E, 24. A frame consists of 24 channels (time-slots) of 8-bit data preceded by an F-bit. Channel data is transmitted and received MSB first.

F-BITS

The use of the F-bit position in 193S is split between the terminal framing pattern (known as F_T-bits) which provides frame alignment information, and the signaling framing pattern (known as F_S-bits) which provides multiframe alignment information. In 193E framing, the F-bit position is shared by the framing pattern sequence (FPS), which provides frame and multiframe alignment information, a 4 KHz data link (facility data link) known as FDL, and CRC (cyclic redundancy check) bits. The FDL bits are used for control and maintenance (inserted by the user at TLINK) and the CRC bits are an indicator of link quality and may be monitored by the user to establish error performance.

SIGNALING

During frames 6 and 12 in 193S, A and B signaling information is inserted into the LSB of all channels transmitted. In 193E, A and B data is inserted into frames 6 and 12, and C and D data is inserted into frames 18 and 24. This allows a maximum of 4 signaling states to be transmitted per superframe in 193S and 16 states in 193E.

ALARMS

The DS2180A supports all alarm pattern generation and detection required in typical Bell System applications. These alarm modes are explained in ATT PUB 43801, ATT C.B. #142 and elsewhere in this document.

5

193E FRAMING FORMAT Table 7

FRAME NUMBER	F-BIT USE			BIT USE IN EACH CHANNEL		SIGNALING-BIT USE		
	FPS[1]	FDL[2]	CRC[3]	DATA	SIGNALING[4,5]	2 STATE	4 STATE	16 STATE
1	—	M	—	BITS 1-8				
2	—	—	C1	BITS 1-8				
3	—	M	—	BITS 1-8				
4	0	—	—	BITS 1-8				
5	—	M	—	BITS 1-8				
6	—	—	C2	BITS 1-7	BIT 8	A	A	A
7	—	M	—	BITS 1-8				
8	0	—	—	BITS 1-8				
9	—	M	—	BITS 1-8				
10	—	—	C3	BITS 1-8				
11	—	M	—	BITS 1-8				
12	1	—	—	BITS 1-7	BIT 8	A	B	B
13	—	M	—	BITS 1-8				
14	—	—	C4	BITS 1-8				
15	—	M	—	BITS 1-8				
16	0	—	—	BITS 1-8				
17	—	M	—	BITS 1-8				
18	—	—	C5	BITS 1-7	BIT 8	A	A	C
19	—	M	—	BITS 1-8				
20	1	—	—	BITS 1-8				
21	—	M	—	BITS 1-8				
22	—	—	C6	BITS 1-8				
23	—	M	—	BITS 1-8				
24	1	—	—	BITS 1-7	BIT 8	A	B	D

NOTES:

1. FPS - Framing Pattern Sequence.
2. FDL - 4 KHz Facility Data Link; M = message bits.
3. CRC - Cyclic Redundancy Check Bits. The CRC code will be internally generated by the device when TCR.5 = 0. When TCR.5 = 1, externally supplied CRC data will be sampled at TSER during the F-bit time of frames 2, 6, 10, 14, 18, 22.
4. The user may program any individual channels clear, in which case Bit 8 will be used for data, not signaling.
5. Depending on application, the user can support 2-state, 4-state or 16-state signaling by the appropriate decodes of TMO, TSIGFR, TSIGSEL (Transmit Side) and RMSYNC, RSIGFR AND RSIGSEL (Receive Side).

193S FRAMING FORMAT Table 8

FRAME NUMBER	F-BIT USE		BIT USE IN EACH CHANNEL		SIGNALING-BIT USE
	$F_T{}^1$	$F_S{}^2$	DATA	SIGNALING[4]	
1	1	—	BITS 1-8		
2	—	0	BITS 1-8		
3	0	—	BITS 1-8		
4	—	0	BITS 1-8		
5	1	—	BITS 1-8		
6	—	1	BITS 1-7	**BIT 8**	A
7	0	—	BITS 1-8		
8	—	1	BITS 1-8		
9	1	—	BITS 1-8		
10	—	1	BITS 1-8		
11	0	—	BITS 1-8		
12	—	0^3	BITS 1-7	**BIT 8**	B

NOTES: 1. F_T (terminal framing) bits provide frame alignment information.
2. F_S (signaling frame) bits provide multiframe alignment information.
3. The S-bit in frame 12 may be used for yellow alarm transmission and detection in some applications.
4. The user may program any individual channels clear, in which case Bit 8 will be used for data, not signaling.

5

LINE CODING

T1 line data is transmitted in a bipolar alternative mark inversion line format; ones are transmitted as alternating negative and positive pulses and zeros are simply the absence of pulses. This technique minimizes DC voltage on the T1 span and allows clock to be extracted from data. The network currently has a one's density constraint to keep clock extraction circuitry functioning, which is usually met by forcing bit 7 of any channel consisting of all 0's to 1. The use of Bipolar Eight Zero Substitution (B8ZS) satisfies all the one's density requirement, while allowing data traffic to be transmitted without corruption. This feature is known as clear channel and is explained more completely in ATT C.B. #144. When the B8ZS feature is enabled, any outgoing stream of eight consecutive zeros is replaced with a B8ZS code word. If the last "one" transmitted was positive, the inserted code is $000 + - 0 - +$; if negative, the code word inserted is $000 - + 0 + -$. Bipolar violations occur in the fourth and seventh bit positions, which are ignored by the DS2180A error monitoring logic when B8ZS is enabled. Any received B8ZS code word is replaced with all 0's if B8ZS is enabled. Also, the receive status register will report any occurrence of B8ZS code words to the host controller. This allows the user to monitor the link for upgrade to clear channel capability, and respond to it. The B8ZS monitoring feature works at all times and is independent of the state of CCR.2.

Transmit Side Overview

The transmit side of the DS2180A is made up of 6 major functional blocks: timing and clock generation, data selector, bipolar coder, yellow alarm, F-bit data and CRC. The timing and clock generation circuit develops all on-board and output clocks to the system from inputs TCLK, TFSYNC and TMSYNC. The yellow alarm circuitry generates mode dependent yellow alarms. The CRC block generates checksum results utilized in 193E framing. F-bit data provides mode dependent framing patterns and allows insertion of link or S-bit data externally. All of these blocks feed into the data selector, where under control of the CCR, TCR, TIRs and TTRs, the contents of the outgoing data stream are established by bit selection and insertion. The bipolar coder formats the output of the data selector to make it compatible with bipolar transmission techniques and inserts zero suppression codes. The bipolar coder also supports the on-board loopback feature. Input to output delay of the transmitter is 10 TCLK cycles.

Receive Side Overview

SYNCHRONIZER

The heart of the receiver is the synchronizer/sync monitor. This circuit serves two purposes: 1) monitoring the incoming data stream for loss of frame or multiframe alignment, and 2) searching for new frame alignment pattern when sync loss is detected. When sync loss is detected, the synchronizer begins an off-line search for the new alignment; all output timing signals remain at the old alignment with the exception of RSIGFR, which is forced low during resync. When one and only one candidate is qualified, the output timing will move to the new alignment at the beginning of the next multiframe. One frame later, RLOS will transition low, indicating valid sync and the resumption of the normal sync monitoring mode. Several bits in the RCR allow tailoring of the resync algorithm by the user. These bits are described below.

SYNC TIME (RCR.2)

Bit RCR.2 determines the number of consecutive framing pattern bits to be qualified before SYNC is declared. If RCR.2 = 1, the algorithm will validate 24 bits; if RCR.2 = 0, 10 bits are validated. 24-bit testing results in superior false framing protection, while 10-bit testing minimizes reframe time (although in either case, the synchronizer will only establish resync when one and only one candidate is found).

RESYNC (RCR.0)

A zero-to-one transition of RCR.0 causes the synchronizer to search for the framing pattern sequence immediately, regardless of the internal sync status. In order to initiate another resync command, this bit must be cleared and then set again.

SYNC ENABLE (RCR.1)

When RCR.1 is cleared, the receiver will initiate automatic resync if any of the following events occur: 1) an OOF event ("out-of-frame"), or 2) carrier loss (32 consecutive 0's appear at RPOS and RNEG). An OOF event occurs any time that 2 of 4 F_T or FPS bits are in error. When RCR.1 is set, the automatic resync circuitry is disabled; in this case, resync can only be initiated by setting RCR.0 to 1, or externally via a low-high transition on $\overline{RST}$. Note that using $\overline{RST}$ to initiate resync resets the receive output timing while $\overline{RST}$ is low; use of RCR.1 does not affect output timing until the new alignment is located.

5

SYNC CRITERIA (RCR.3)

193E

Bit RCR.3 determines which sync algorithm is utilized when resync is in progress (RLOS = 1). In 193E framing, when RCR.3 = 0, the synchronizer will lock only to the FPS pattern and will move to the new frame and multiframe alignment after the framing candidate is qualified. RLOS will go low one frame after the move to the new alignment. When RCR.3 = 1, the new alignment is further tested by a CRC code match. RLOS will transition low after a CRC match occurs. If no CRC match occurs in three attempts (three multiframes), the algorithm will reset and a new search for the framing pattern begins. It takes 9 ms for the synchronizer to check the first CRC code after the new alignment has been loaded. Each additional CRC test takes 3 msec. Regardless of the state of RCR.3, if more than one candidate exists after about 24 milliseconds, the synchronizer will begin eliminating emulators by testing their CRC codes on-line in order to find the true framing candidate.

193S

In 193S framing, when RCR.3 = 1, the synchronizer will cross check the F_T pattern with the F_S pattern to help eliminate false framing candidates such as digital milliwatts. The F_S patterns are compared to the repeating pattern . . . 00111000111000 . . . (00111X0 if CCR.3—YELMD—is equal to a 1).In this mode, F_T and F_S patterns must be correctly identified by the synchronizer before sync is declared. Clearing RCR.3 causes the synchronizer to search for F_T patterns (101010 . . .) without cross-coupling the F_S pattern. Frame sync will be established using the F_T information, while multiframe sync will be established only if valid F_S information is present. If no valid F_S pattern is identified, the synchronizer will move to the F_T alignment, RLOS will go low, and a false multiframe position may be indicated by RMSYNC. RFER will indicate when the received S-bit pattern does not match the assumed internal multiframe alignment. This mode will be used in applications where non-standard S-bit patterns exist. In such applications multiframe alignment information can be decoded externally by using the S-bits present at RLINK.

AVERAGE REFRAME TIME[1] Table 9

FRAME MODE	RCR.2 = 0			RCR.2 = 1			UNITS
	MIN	AVG	MAX	MIN	AVG	MAX	
193S	3.0	3.75	4.5	6.5	7.25	8.0	msec
193E	6.0	7.5	9.0	13.0	14.5	16.0	

NOTES: 1. Average Reframe Time is defined here as the average time it takes from the start of resync (rising edge of RLOS) to the actual loading of the new alignment (on a multiframe edge) into the output receive timing.
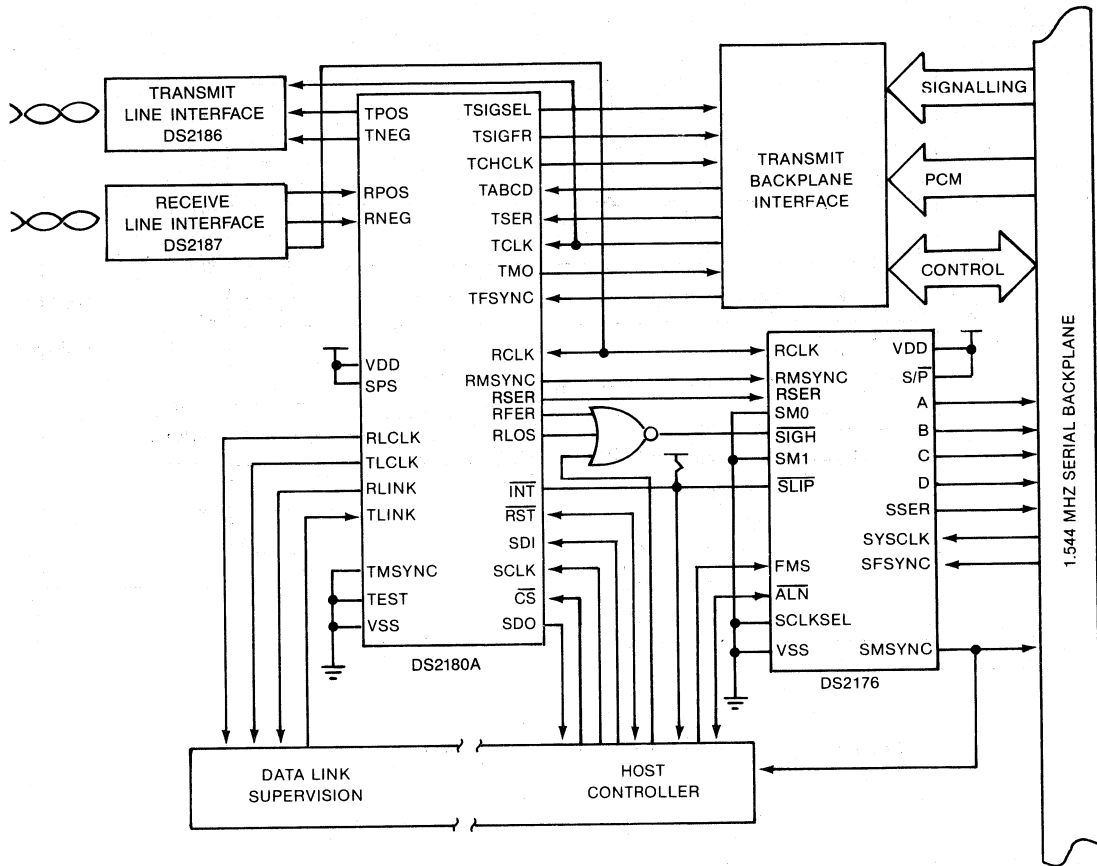
PROCESSOR-BASED TRANSMIT SIGNALLING INSERTION Figure 23
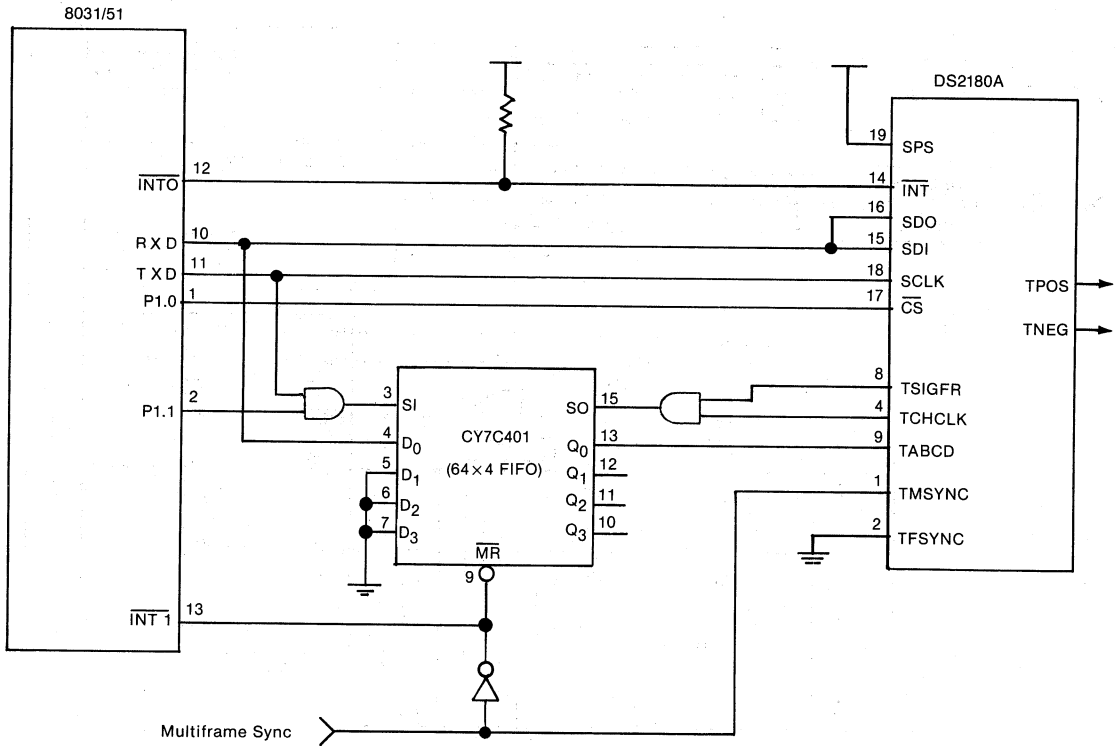
PROCESSOR-BASED SIGNALING
Many robbed-bit signaling applications utilize a microprocessor to insert transmit signaling data into the outgoing data stream. The circuit shown in figure 23 "decouples" the processor timing from that of the DS2180A by use of a small FIFO memory. The processor writes to the FIFO (6 bytes are written: 3 for A data, 3 for B data) only when signaling updates are required. The FIFO automatically retransmits old data when no updates occur. The system is interrupt-driven from the transmit multiframe sync input; the processor must update the FIFO prior to Frame 6 (625 *us*) after interrupt) to prevent data corruption. The application circuit shown supports 193S framing; additional hardware is required for 193E applications.

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	—	$-1.0V$ to $+7V$
OPERATING TEMPERATURE	—	0°C to 70°C
STORAGE TEMPERATURE	—	-55°C to 125°C
SOLDERING TEMPERATURE	—	260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS · (0 °C to 70 °C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS
Logic 1	V_{IH}	2.0		$V_{DD} + .3$	V
Logic 0	V_{IL}	-0.3		$+0.8$	V
Supply	V_{DD}	4.5	5.0	5.5	V

CAPACITANCE ($t_A = 25$ °C)

PARAMETER	SYMBOL	MAX	UNITS
Input Capacitance	C_{IN}	5	pF
Output Capacitance	C_{OUT}	7	pF

D.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C $V_{DD} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Supply Current	I_{DD}		3	10	mA	1,2
Input Leakage	I_{IL}			1	µA	
Output Leakage	I_{LO}			1	µA	3
Output Current @ 2.4V	I_{OH}	-1			mA	4
Output Current @ .4V	I_{OL}	$+4$			mA	5

NOTES: 1. TCLK = RCLK = 1.544 MHz
2. Outputs open
3. Applies to SDO when tristated
4. All outputs except $\overline{INT}$, which is open collector
5. All outputs

A.C. ELECTRICAL CHARACTERISTICS[1] — SERIAL PORT   (0 °C to 70 ° V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS
SDI to SCLK Set up	t_{DC}	50			ns
SCLK to SDI Hold	t_{CDH}	50			ns
SDI to SCLK Falling Edge	t_{CD}	50			ns
SCLK Low Time	t_{CL}	250			ns
SCLK High Time	t_{CH}	250			ns
SCLK Rise & Fall Time	t_R, t_F			500	ns
$\overline{CS}$ to SCLK Set Up	t_{CC}	50			ns
SCLK to $\overline{CS}$ Hold	t_{CCH}	50			ns
$\overline{CS}$ Inactive Time	t_{CWH}	250			ns
SCLK to SDO Valid[2]	t_{CDV}			200	ns
$\overline{CS}$ to SDO High Z	t_{CDZ}			75	ns
SCLK Setup to $\overline{CS}$ Falling	t_{SSC}	50			ns

NOTES:
1. Measured at V_{IH} = 2.0V, V_{IL} = .8V, and 10 ns maximum rise and fall time.
2. Output load capacitance = 100 pF.

SERIAL PORT WRITE A.C. TIMING DIAGRAM
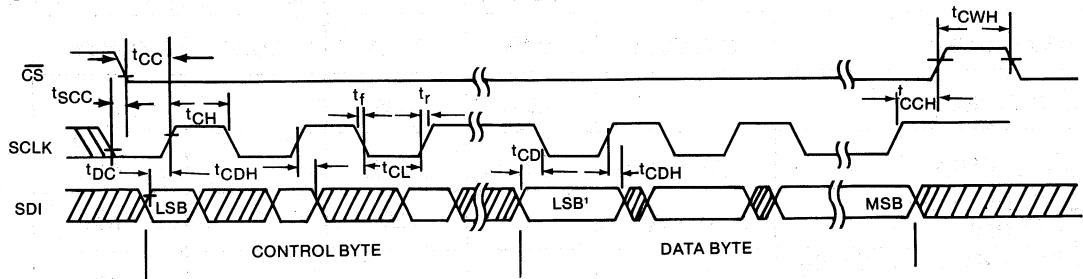
NOTES: 1. Data byte bits must be valid across low clock periods to prevent transients in operating modes.

2. Shaded regions indicate don't-care states of input data.

SERIAL PORT READ[1] A.C. TIMING
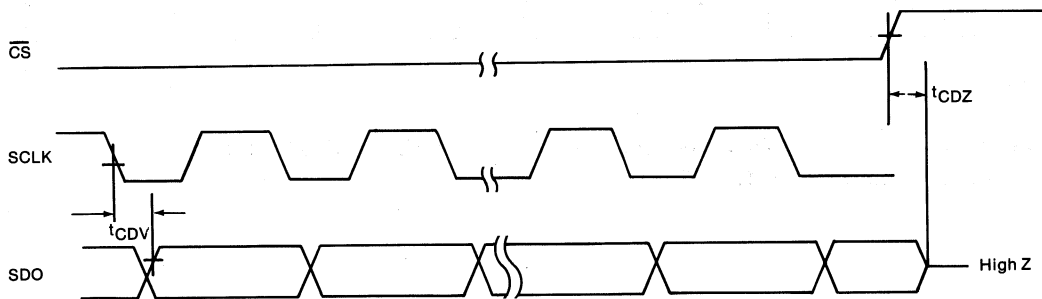
NOTES: 1. Serial port write must precede a port read to provide address information.

A.C. ELECTRICAL CHARACTERISTICS[1] — TRANSMIT   (0 °C to 70°, $V_{DD} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS
TCLK Period	t_P	250	648		ns
TCLK Pulse Width	t_{WL}, t_{WH}	125	324		ns
TCLK, RCLK Rise & Fall Times	t_F, t_R		20		ns
TSER, TABCD, TLINK Set Up to TCLK Falling	t_{STD}	50			ns
TSER, TABCD, TLINK Hold from TCLK Falling	t_{HTD}	50			ns
TFSYNC, TMSYNC Set Up to TCLK Rising	t_{STS}	−125		125	ns
Propagation Delay TFSYNC to TMO, TSIGSEL, TSIGFR, TLCLK	t_{PTS}			75	ns
Propagation Delay TCLK to TCHCLK	t_{PTCH}			75	ns
TFSYNC, TMSYNC Pulse Width	t_{TSP}	100			ns

NOTES:

1. Measured at $V_{IH} = 2.0V$, $V_{IL} = .8V$, and 10 ns maximum rise and fall time.
2. Output load capacitance = 100 pF.

A.C. ELECTRICAL CHARACTERISTICS[1] — RECEIVE (0 °C to 70 °, V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS
Propagation Delay RCLK to RMSYNC, RFSYNC, RSIGSEL, RSIGFR, RLCLK, RCHCLK	t_{PRS}			75	ns
Propagation Delay RCLK to RSER, RABCD, RLINK	t_{PRD}			75	ns
Transition Time All Outputs	t_{TTR}			20	ns
RCLK Period	t_P	250	648		ns
RCLK Pulse Width	t_{WL}, t_{WH}	125	324		ns
RCLK Rise & Fall Times	t_R, t_F		20		ns
RPOS, RNEG Set Up to RCLK Falling	t_{SRD}	50			ns
RPOS, RNEG Hold to RCLK Falling	t_{HRD}	50			ns
Propagation Delay RCLK to RYEL, RCL, RFER, RLOS, RBV	t_{PRA}			75	ns
Minimum RST Pulse Width on System Power Up or Restart	t_{RST}	1			μs

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NOTES:

1. Measured at V_{IH} = 2.0 V, V_{IL} = .8V, and 10 ns maximum rise and fall time.
2. Output load capacitance = 100 pF.

TRANSMIT A.C. TIMING DIAGRAM

TCLK

TSER, TABCD, TLINK

TFSYNC, TMSYNC

TMO, TLCLK, TSIGSEL, TSIGFR

TCHCLK

RECEIVE A.C. TIMING DIAGRAM

RCLK

RSER, RABCD RLINK

RMSYNC, RFSYNC RSIGSEL, RSIGFR RLCLK, RCHCLK

RYEL, RCL, RBV RFER, RLOS

RST

RPOS, RNEG
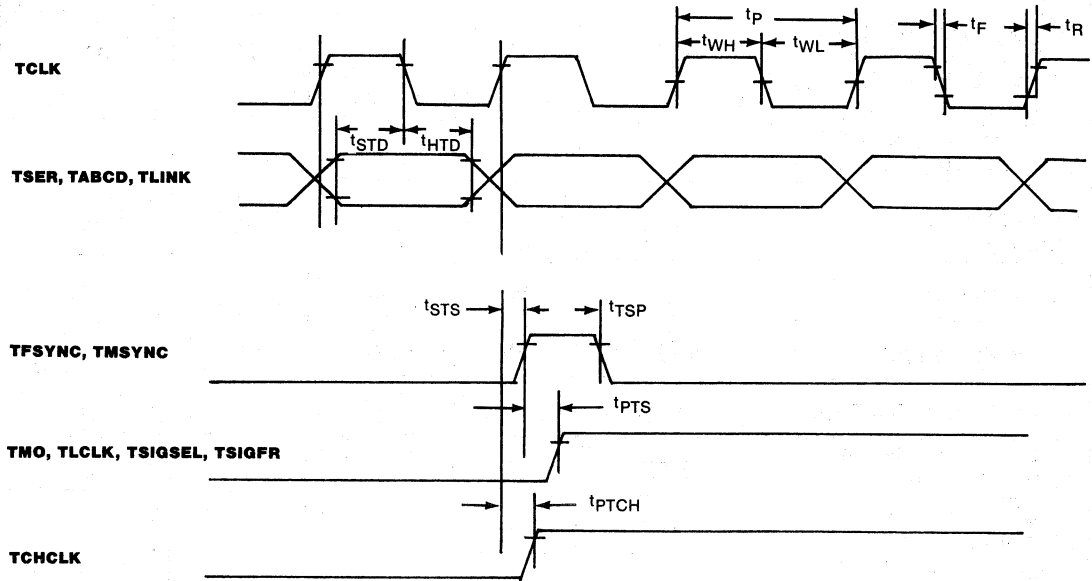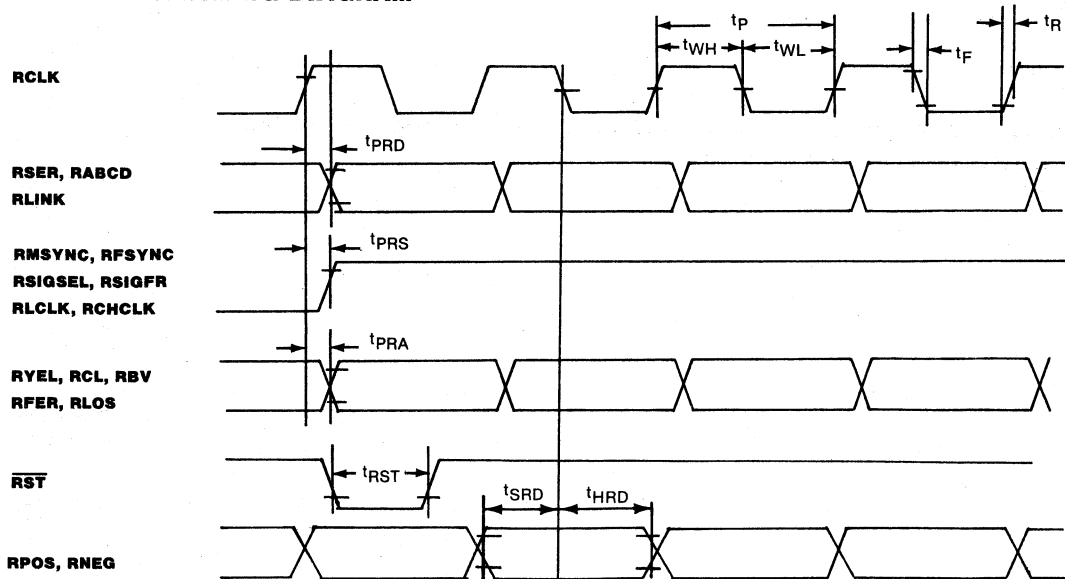
DS2180A
Serial T1 Transceiver
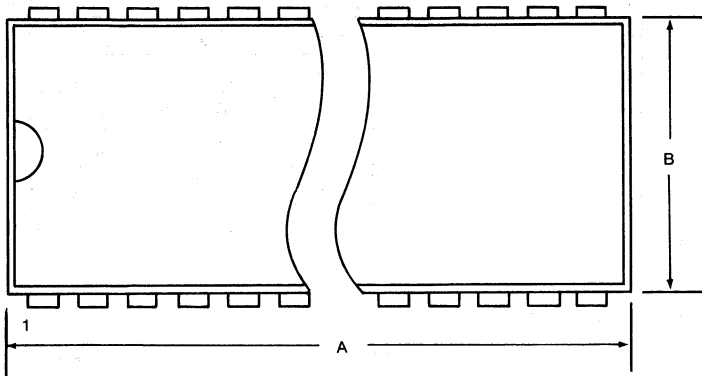
DIM.	INCHES	
	MIN.	MAX.
A	2.040	2.080
B	.540	.560
C	.140	.160
D	.590	.610
E	.020	.040
F	.110	.130
G	.090	.110
H	.600	.680
J	.008	.012
K	.015	.021

5

19 EQUAL SPACES AT
.100 ± .010 TNA
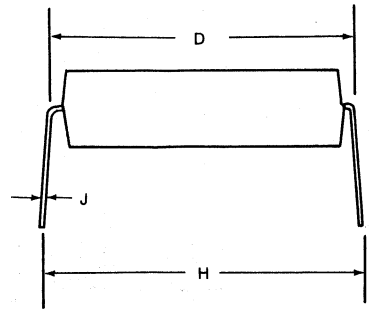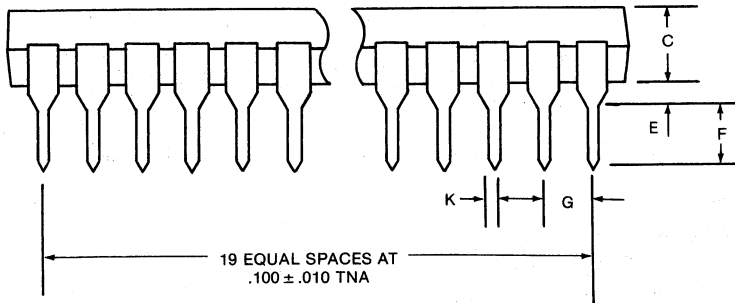
DS2180AQ

DIM.	INCHES	
	MIN.	MAX.
A	.490	.510
B	.590	.630
C	.020	.024
D	.018	.022
E	.688	.692
F	.118	.122
G	.020	.030
H	.590	.630
I	.167	.173
J	.048	.051

45°

Pin No. 1

.010R
(3×)

A

B

J

C

E

D

D

F

G

.010 MAX.

0-5 DEG

H

Top pins (left to right): N.C., TCHCLK, TCLK, N.C., TFSYNC, TMSYNC, VDD, RLOS, RFER, RBV, RCL

Left pins (top to bottom): TSER, TMO, TSIGSEL, TSIGFR, TABCD, TLINK, TLCLK, TPOS, TNEG, INT, SDI

Right pins (top to bottom): RNEG, RPOS, RST, TEST, RSIGSEL, RSIGFR, RABCD, RMSYNC, RFSYNC, RSER, RCHCLK

Bottom pins (left to right): SDO, CS, SCLK, SPS, VSS, RYEL, RLINK, N.C., RLCLK, RCLK, N.C.
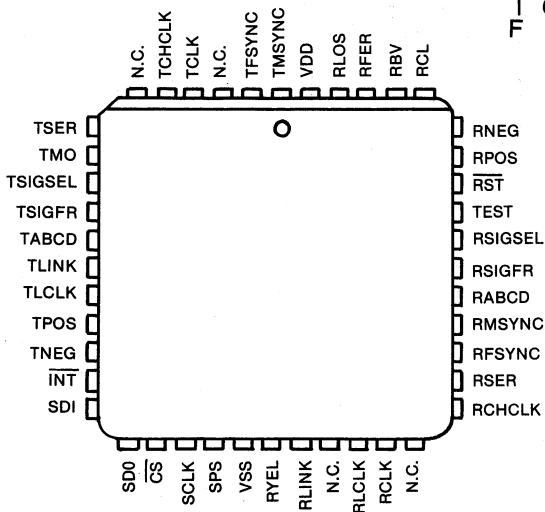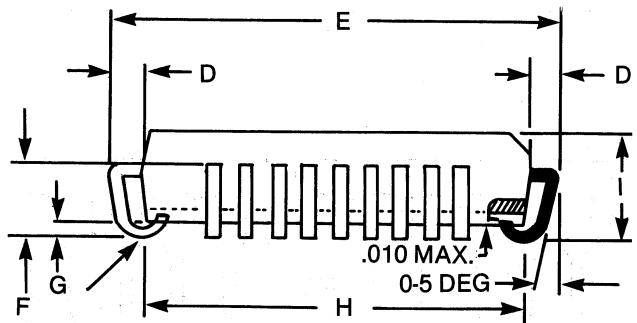
Dallas Semiconductor
CEPT PRIMARY RATE TRANSCEIVER

FEATURES
● Single chip primary rate transceiver
  meets CCITT standards: G.704
  and G.732

● Supports new CRC4 based framing
  standards and CAS and CCS signalling
  standards

● Simple serial interface used for device
  configuration and control in
  "processor" mode

● "Hardware" mode requires no host
  processor; intended for stand-alone
  applications

● Comprehensive on-chip alarm
  generation, alarm detection and
  error logging logic

● Shares footprint with DS2180A
  T1 Transceiver

● Companion to DS2175 Transmit/Receive
  Elastic Store

● 5V supply, low power CMOS technology

PIN CONNECTIONS

TMSYNC	1	40 VDD
TFSYNC	2	39 RLOS
TCLK	3	38 RFER
TCHCLK	4	37 RBV
TSER	5	36 RCL
TMO	6	35 RNEG
TXD	7	34 RPOS
TSTS	8	33 RST
TSD	9	32 TEST
TIND	10	31 RCSYNC
TAF	11	30 RSTS
TPOS	12	29 RSD
TNEG	13	28 RMSYNC
INT	14	27 RFSYNC
SDI	15	26 RSER
SDO	16	25 RCHCLK
CS	17	24 RCLK
SCLK	18	23 RAF
SPS	19	22 RDMA
VSS	20	21 RRA

DESCRIPTION
The DS2181 is designed for use in CEPT net-
works and supports all logical requirements of
CCITT Red Book Recommendations G.704 and
G.732. The transmit side generates framing
patterns and CRC4 codes, formats outgoing
channel and signalling data and produces net-
work alarm codes when enabled. The receive
side decodes the incoming data and establishes
frame, CAS multiframe, and CRC4 multiframe
alignments. Once synchronized, the device ex-
tracts channel, signalling and alarm data.

A serial port allows access to 14 on-chip control
and status registers in the processor mode. In
this mode, a host processor controls such fea-
tures such as error logging, per-channel code
manipulation and alteration of the receive syn-
chronizer algorithm.

The hardware mode is intended for preliminary
system prototyping and/or retrofitting into exist-
ing systems. This mode requires no host proces-
sor and disables special features available in the
processor mode.

DS2181 BLOCK DIAGRAM Figure 1
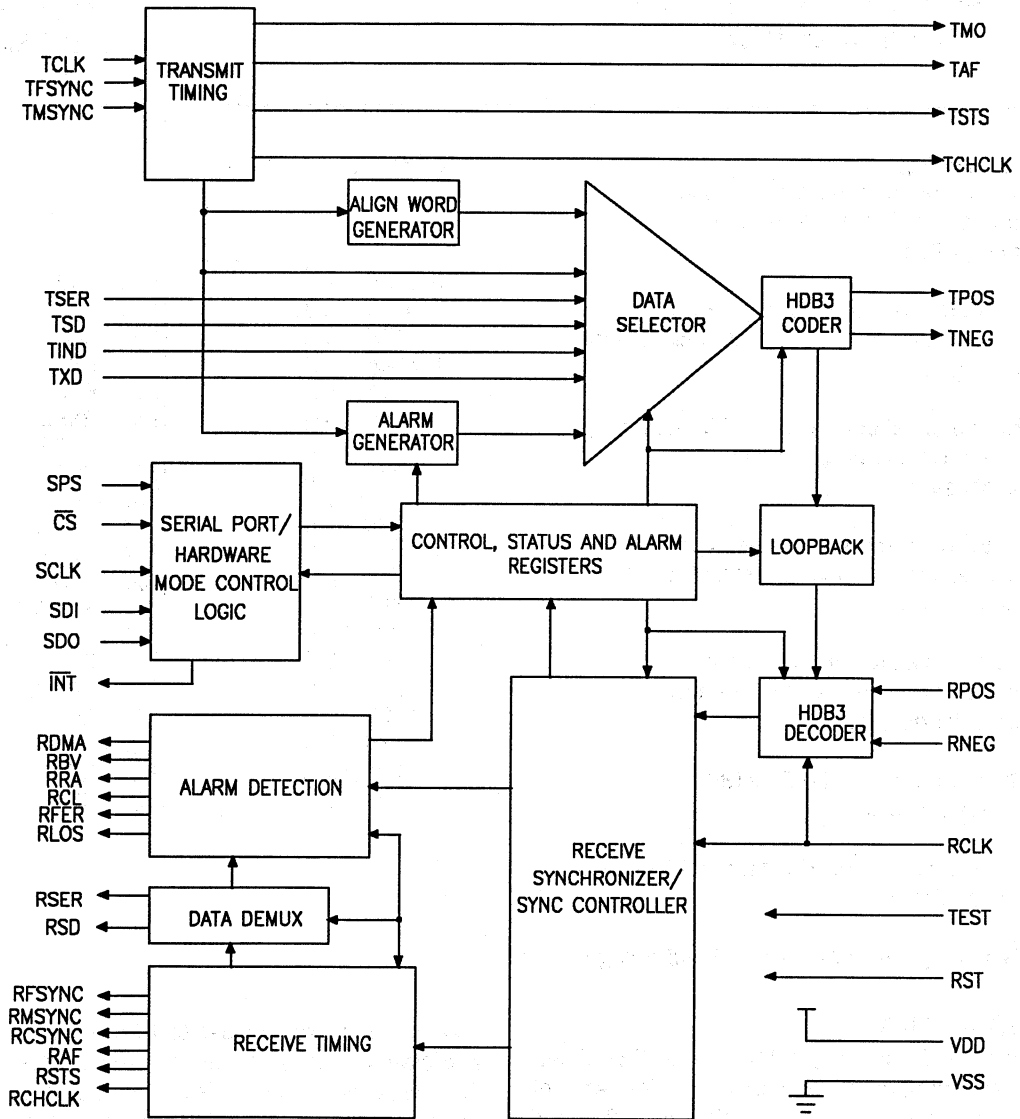
TRANSMIT PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	TMSYNC	I	**Transmit Multiframe Sync.** Low-high transition establishes start of CAS and/or CRC4 multiframe. May be tied low, allowing internal multiframe counter to run free.
2	TFSYNC	I	**Transmit Frame Sync.** Low high transition every frame period establishes frame boundaries. May be tied low, allowing TMSYNC to establish frame boundaries.
3	TCLK	I	**Transmit Clock.** 2.048 MHz primary clock.
4	TCHCLK	O	**Transmit Channel Clock.** 256 KHz clock which identifies timeslot boundries. Useful for parallel to serial conversion of channel data.
5	TSER	I	**Transmit Serial Data.** NRZ data input, sampled on falling edges of TCLK.
6	TMO	O	**Transmit Multiframe Out.** Output of multiframe counter, high during frame 0, low otherwise.
7	TXD	I	**Transmit Extra Data.** Sampled on falling edge of TCLK during bit times 5, 7, and 8 of timeslot 16 in frame 0 when CAS signalling is enabled.
8	TSTS	O	**Transmit Signalling Timeslot.** High during timeslot 16 of every frame, low otherwise.
9	TSD	I	**Transmit Signalling Data.** CAS signalling data input; sampled on falling edges of TCLK for insertion into outgoing timeslot 16 when enabled.
10	TIND	I	**Transmit International and National Data.** Sampled on falling edge of TCLK during bit 1 time of timeslot 0 every frame (international) and/or during bit times 4 thru 8 of timeslot 0 during non-align frames (national) when enabled.
11	TAF	O	**Transmit Alignment Frame.** High during frames containing the frame alignment signal, low otherwise.
12 13	TPOS TNEG	O	**Transmit Bipolar Data Outputs.** Updated on rising edge of TCLK.

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RECEIVE PIN DESCRIPTION Table 2

PIN	SYMBOL	TYPE	DECRIPTION
21	RRA	O	**Receive Remote Alarm.** Transitons high when alarm detected, returns low when alarm cleared.
22	RDMA	O	**Receive Distant Multiframe Alarm.** Transitions high when alarm detected, returns low when alarm cleared.
23	RAF	O	**Receive Alignment Frame.** High during frames containing the frame alignment signal, low otherwise.
24	RCLK	I	**Receive Clock.** 2.048 MHz primary clock.
25	RCHCLK	O	**Receive Channel Clock.** 256 KHz clock, identifies timeslot boundries; useful for serial to parallel conversion of channel data.
26	RSER	O	**Receive Serial Data.** Received NRZ data, updated on rising edges of RCLK.
27	RFSYNC	O	**Receive Frame Sync.** Trailing edge indicates start of frame.
28	RMSYNC	O	**Receive Multiframe Sync.** Low-high transition indicates start of CAS multiframe, held high during frame 0.
29	RSD	O	**Receive Signaling Data.** Extracted timeslot 16 data, updated on rising edge of RCLK.
30	RSTS	O	**Receive Signaling Timeslot.** High during timeslot 16 of every frame, low otherwise.
31	RCSYNC	O	**Receive CRC4 Sync.** Low-high transition indicates start of CRC4 multiframe, held high during CRC4 frames 0 thru 7 and held low during frames 8 through 15.
33	$\overline{\text{RST}}$	I	**Reset.** Must be asserted during device power-up and when changing to/from the hardware mode.
34 35	RPOS RNEG	I	**Receive Bipolar Data.** Sampled on falling edges of RCLK.
36	RCL	O	**Receive Carrier Loss.** Low-high transition indicates loss of carrier.

37	RBV	O	**Receive Bipolar Violation.** Pulses high during detected bipolar violations.
38	RFER	O	**Receive Frame Error.** Pulses high when frame alignment, CAS multiframe alignment or CRC4 words received in error.
39	RLOS	O	**Receive Loss of Sync.** Indicates synchronizer status; high when frame, CAS and/or CRC4 multiframe search underway, low otherwise.

PORT PIN DESCRIPTION Table 3

PIN	SYMBOL	TYPE	DESCRIPTION
14	$\overline{\text{INT}}$	O	**Receive Alarm Interrupt.** Flags host controller during alarm conditions. Active low, open drain output.
15	SDI	I	**Serial Data In.** Data for on-chip control registers; sampled on rising edge of SCLK.
16	SDO	O	**Serial Data Out.** Control and status data from on-chip registers. Updated on falling edge of SCLK, tristated during port write or when CS is high.
17	$\overline{\text{CS}}$	I	**Chip Select.** Must be low to write or read the serial port.
18	SCLK	I	**Serial Data Clock.** Used to write or read the serial port registers.
19	SPS	I	**Serial Port Select.** Tie to VDD to select the serial port. Tie to VSS to select the hardware mode.

POWER AND TEST PIN DESCRIPTION Table 4

PIN	SYMBOL	TYPE	DESCRIPTION
20	VSS	-	**Signal Ground.** 0.0 volts.
32	TEST	I	**Test Mode.** Tie to VSS for normal operation.
40	VDD	-	**Positive Supply.** 5.0 volts.

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REGISTER SUMMARY Table 5

REGISTER	ADDRESS	T/R[1]	DESCRIPTION/FUNCTION
RIMR	0000	R	**Receive Interrupt Mask Register.** Allows masking of alarm generated interrupts.
RSR	0001	R[2]	**Receive Status Register.** Reports all receive alarm conditions.
BVCR	0010	R	**Bipolar Violation Count Register.** 8 bit presettable counter which records individual bipolar violations.
CECR	0011	R	**CRC4 Error Count Register.** 8 bit presettable counter which records individual CRC4 errors.
FECR	0100	R	**Frame Error Count Register.** 8 bit presettable counter which logs individual errors in the received frame alignment signal.
RCR	0101	R	**Receive Control Register.** Establishes receive side operating characteristics.
CCR	0110	T/R	**Common Control Register.** Establishes additional operating characteristics for transmit and receive sides.
TCR	0111	T	**Transmit Control Register.** Establishes transmit side operation characteristics.
TIR1 TIR2 TIR3 TIR4	1000 1001 1010 1011	T	**Transmit Idle Registers** Designates which outgoing timeslots are to be substituted with idle code.
TINR	1100	T	**Transmit International and National Register.** When enabled via the TCR, contents inserted into the outgoing national and/or international bit positions.
TXR	1101	T	**Transmit Extra Register.** When enabled via the TCR, contents inserted into the outgoing extra bit positions.

NOTES:
1. Transmit or receive side register.
2. RSR is a read only register, all other registers are read/write.
3. Reserved bit locations must be programmed to zero.

SERIAL PORT INTERFACE

Pins 14 thru 18 of the DS2181 serve as a microprocessor/microcontroller compatible serial port. 14 on-chip registers allow the user to update operational characteristics and monitor device status via a host controller, minimizing hardware interfaces.

Port read/write timing is unrelated to the chip transmit and receive timing, allowing asynchronous reads and/or writes by the host. The timing set is identical to that of "8051 type" microcontrollers operating in serial port mode 0. For proper operation of the port and the transmit and receive registers, the user should provide TCLK and RCLK as well as SCLK.

ADDRESS/COMMAND

An address/command byte write must precede any read or write of the port registers. The first bit written (LSB) of the address/command byte specifies read or write. The following nibble identifies register address. The next two bits are reserved and must be set to zero for proper operation. The last bit of the address/command word enables the burst mode when set; the burst mode allows consecutive reading or writing of all register data. *Data is written to and read from the port LSB first.*

CHIP SELECT AND CLOCK CONTROL

All data transfers are initiated by driving the CS input low. Data is sampled on the rising edge of SCLK and must be valid during the previous low period of SCLK to prevent momentary corruption of written register contents. Data is output on the falling edge of SCLK and held to the next falling edge. All data transfers are terminated and SDO tristated when CS returns to high.

CLOCKS

To access the serial port registers both TCLK and RCLK are required along with the SCLK. The TCLK and RCLK are used to access internally the transmit and receive registers respectively. The CCR is considered a receive register for this purpose.

DATA I/O

Following the 8 SCLK cycles that input the address/command byte, data at SDI is strobed into the addressed register on the next 8 SCLK cycles (register write) or data is presented at SDO on the next 8 SCLK cycles (register read). SDO is tristated during writes and may be tied to SDI in applications where the host processor has bidirectional I/O capability.

BURST MODE

The burst mode allows all on-chip registers to be consecutively read or written by the host processor. This feature minimizes device initialization time on system power-up or reset. Burst mode is initiated when ACB.7 is set and the address nibble is 0000. *All registers must be read or written during the burst mode. If CS transitions high before the burst is complete, data validity is not guaranteed.*

ACB: ADDRESS COMMAND BYTE Figure 2

(MSB)   (LSB)

BM	- -	- -	ADD3	ADD2	ADD1	ADD0	R/W
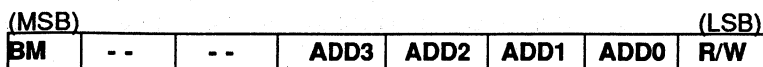
SYMBOL	POSITION	NAME AND DESCRIPTION
BM	ACB.7	**Burst Mode.** If set (and ACB.1 thru ACB.4 = 0) burst read or write is enabled.
- -	ACB.6	Reserved, must be 0 for proper operation.
- -	ACB.5	Reserved, must be 0 for proper operation.
ADD3	ACB.4	MSB of register address.
ADD2	ACB.3	
ADD1	ACB.2	
ADD0	ACB.1	LSB of register address.
R/W	ACB.0	**Read/Write select.** 0 = Write addressed register. 1 = Read addressed register.

SERIAL PORT READ/WRITE Figure 3
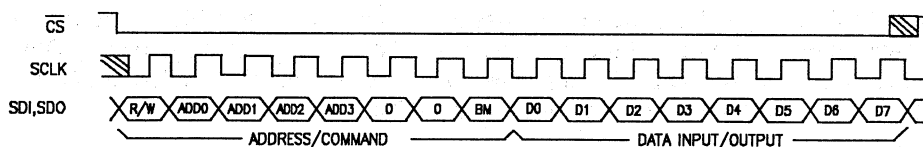
NOTES:
1. SDI sampled on rising edge of SCLK.
2. SDO updated on falling edge of SCLK.

TCR: TRANSMIT CONTROL REGISTER Figure 4

(MSB)   (LSB)

TUA1	TSS	TSM	INBS	NBS	XBS	TSA1	ODM

SYMBOL	POSITION	NAME AND DESCRIPTION
TUA1	TCR.7	**Transmit Unframed All 1s** 0 = Normal operation. 1 = Replace outgoing data at TPOS and TNEG with unframed all 1s code.
TSS	TCR.6	**Transmit Signalling Select[1]** 0 = Signalling data embedded in the serial bit stream is sampled at TSER during timeslot 16. 1 = Signalling data is channel associated and sampled at TSD as shown in Table 6.
TSM	TCR.5	**Transmit Signalling Mode[1]** 0 = Channel Associated Signalling (CAS) 1 = Common Channel Signalling (CCS)
INBS	TCR.4	**International Bit Select** 0 = Sample international bit at TIND 1 = Outgoing international bit = TINR.7
NBS	TCR.3	**National Bit Select** 0 = Sample national bits at TIND 1 = Source outgoing national bits from TINR.4 thru TINR.0
XBS	TCR.2	**Extra Bit Select** 0 = Sample extra bits at TXD 1 = Source extra bits from TXR.0 thru TXR.1 and TXR.3
TSA1	TCR.1	**Transmit Signalling All "1s"** 0 = Normal operation 1 = Force contents of timeslot 16 in all frames to all "1s"
ODM	TCR.0	**Output Data Mode** 0 = TPOS and TNEG outputs are 100% duty cycle. 1 = TPOS and TNEG outputs are 50% duty cycle.

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NOTE:
1. When the common channel signalling mode is enabled (TCR.5 = 1), the TSD input is disabled internally; all timeslot 16 data is sampled at TSER.

CCR: COMMON CONTROL REGISTER Figure 5

(MSB)							(LSB)
- -	TAFP	THDE	RHDE	TCE	RCE	- -	LLB

SYMBOL	POSITION	NAME AND DESCRIPTION
- -	CCR.7	Reserved, must be 0 for proper operation.
TAFP	CCR.6	**Transmit Align Frame Position**[1] When clear, the CAS multiframe begins with a frame containing the frame alignment signal. When set, the CAS multiframe begins with a frame not containing the frame alignment signal.
THDE	CCR.5	**Transmit HDB3 Enable** 0 = Outgoing data at TPOS and TNEG is AMI coded. 1 = Outgoing data at TPOS and TNEG is HDB3 coded.
RHDE	CCR.4	**Receive HDB3 Enable** 0 = Incoming data at RPOS and RNEG is AMI coded. 1 = Incoming data at RPOS and RNEG is HDB3 coded.
TCE	CCR.3	**Transmit CRC4 Enable** When set, outgoing international bit positions in frames 0 thru 12 and 14 are replaced by CRC4 multiframe alignment and checksum words.
RCE	CCR.2	**Receive CRC4 Enable** 0 = Disable CRC4 multiframe synchronizer 1 = Enable CRC4 synchronizer, search for CRC4 multiframe alignment once frame alignment complete.
- -	CCR.1	Reserved, must be 0 for proper operation.
LLB	CCR.0	**Local Loopback** 0 = Normal operation 1 = Internally loop TPOS, TNEG and TCLK to RPOS, RNEG and RCLK.

NOTES
1. This bit must be cleared when CRC4 multiframe mode is enabled (CCR.3 = 1); its state does not affect CCS framing (RCR.5 = 1).
2. CCR is considered a receive register and operates from RCLK and SCLK

RCR: RECEIVE CONTROL REGISTER Figure 6

- -	- -	RSM	CMRC	CMSC	FRC	SYNCE	RESYNC

SYMBOL	POSITION	NAME AND DESCRIPTION
- -	RCR.7	Reserved, must be 0 for proper operation.
- -	RCR.6	Reserved, must be 0 for proper operation.
RSM	RCR.5	**Received Signalling Mode** 0 = Channel Associated Signalling (CAS) 1 = Common Channel Signalling (CCS)
CMSC	RCR.4	**CAS Multiframe Sync Criteria** 0 = Declare sync when fixed sync criteria met 1 = Declare sync when fixed criteria are met and two additional consecutive valid multiframe alignment signals are detected
CMRC	RCR.3	**CAS Multiframe Resync Criteria** 0 = Utilize only fixed resync criteria 1 = Resync if fixed criteria met and/or if two consecutive timeslot 16 words have values of zero in the first four MSB positions (0000xxxx)
FRC	RCR.2	**Frame Resync Criteria** 0 = Utilize only fixed resync criteria 1 = Resync if fixed criteria met and/or if bit 2 in timeslot 0 of non-align frames is received in error on 3 consecutive occasions
SYNCE	RCR.1	**Sync Enable** If clear, the synchronizer will automatically begin resync if error criteria are met. If high, no auto resync occurs
RESYNC	RCR.0	**Resync** When toggled low to high, the receive synchronizer will initate immediately. The bit must be cleared, then set again for subsequent resyncs

5

CEPT FRAME STRUCTURE

The CEPT frame is made up of 32 8-bit channels (timeslots) numbered from 0 to 31. The frame alignment signal in bit positions 2 thru 8 of timeslot 0 of every other frame is independent of the various multiframe modes described below. Outputs TAF and RAF indicate frames which contain the alignment signal. Timeslot 0 of frames not containing the frame alignment signal is used for alarm and national data.

CAS SIGNALING

CEPT networks support Channel Associated Signalling (CAS) or Common Channel Signalling (CCS). These signalling modes are independently selectable for transmit and receive sides.

CAS (selected when TCR.5 = 0 and/or when RCR.5 = 0) is a bit oriented signalling technique which utilizes a 16 frame multiframe. The multiframe alignment signal (0-hex), extra and alarm bits occupy timeslot 16 of frame 0. Timeslot 16 of the remaining 15 frames is reserved for channel signalling data. Four signalling bits (A, B, C and D) are transmitted once per multiframe as shown in Figure 7. Input TMSYNC establishes the transmitted CAS multiframe position. Signalling data may be sourced from input TSD (TCR.6 = 1) or multiplexed into TSER (TCR.6 = 0).

CCS SIGNALLING

CCS (selected whtn TCR.5 = 1 and/or when RCR.1 = 1) utilizes all bit positions of timeslot 16 in every frame for "message oriented" signalling data transmission. In CCS mode one can use either timeslot 16 or any one of the other 30 data channels for message oriented signalling. The CCS mode has no multiframe structure and the insertion of CAS multiframe alignment, distant multiframe alarm and/or extra bits into timeslot 16 is disabled. TSER is the source of timeslot 16 data.

CRC4 CODING

The need for enhanced error monitoring capability and additional protection against emulators of the frame alignment word has let to the development of a cyclic redundancy check (CRC) procedure. When enabled via CCR.2 and/or CCR.3, CRC4 coding reploaces the international bit positions in frames 0 thru 12 and 14 with a CRC4 multiframe alignment pattern and associated checksum words. The CRC4 multiframe must begin with a frame containing the frame alignment signal (CCR.6 = 0). A rising edge at TMSYNC establishes the CRC4 multiframe alignment (TMSYNC will also establish outgoing CAS multiframe alignment if enabled via TCR.5).

Incoming CRC4 multiframe alignment is indicated by RCSYNC. Detected CRC4 checksum errors are reported at output RFER and logged in the CECR.

RECEIVE SYNCHRONIZER

The fixed characteristics of the receive synchronizer may be modified by use of programmable characteristics resident in the RCR and CCR. Sync criteria must be met before synchronization is declared. Resync criteria establish error occurrences which will cause an auto-resync event when enabled (RCR.1 = 0).

The receive synchronizer searches for the frame alignment pattern first. Once identified, the output timing set associated with the framing pattern (all outputs except RCSYNC) is updated to that new alignment. If enabled, the synchronizer then begins CAS and/or CRC4 multiframe search, outputs RMSYNC and/or RCSYNC are then updated. Output RLOS is held high during the entire resync process, then transitions low after the last output timing update indicating resync is complete.

FIXED FRAME SYNC CRITERIA

Valid frame sync is assumed when the correct frame alignment signal is present in frame N and frame N + 2 and not present in frame N + 1 (Bit 2 of Timeslot 0 of Frame N + 1 is also checked for "1"). CAS and/or CRC4 multiframe alignment search is initiated when the frame search is complete if enabled via RCR.5 and/or CCR.2

FIXED CAS MULTIFRAME SYNC CRITERIA

CAS multiframe sync is declared when the multiframe alignment pattern is properly detected and timeslot 16 of the previous frame contains code other than zeros. If no valid pattern can be found in 12 to 14 milliseconds, frame search is restarted.

FIXED CRC4 MULTIFRAME SYNC CRITERIA

CRC4 multiframe sync is declared if at least two valid CRC4 multiframe alignment signals are found within 12 to 14 milliseconds after frame alignment is completed. If not found within 12 to 14 milliseconds, frame search is restarted. The search for the multiframe alignment signal is performed in timeslot 0 of frames not containing the frame alignment signal.

FIXED FRAME RESYNC CRITERIA

When enabled via RCR.1, the device will automatically initiate frame search whenever the frame alignment word is received in error three consecutive times.

FIXED CAS MULTIFRAME RESYNC CRITERIA

When enabled via RCR.1, the device will automatically initiate frame search whenever two consecutive CAS multiframe alignment words are received in error.

FIXED CRC4 MULTIFRAME RESYNC CRITERIA

When enabled via RCR.1, the device will automatically initiate frame search whenever 64 or fewer individual CRC4 bits of the last 1024 CRC4 words are received without error. Even when the incoming CRC4 code words are random in data, the probability that 64 bits are good out of 1024 words (4096 bits) is almost 100%. The threshold for the CRC4 Multiframe Resync Criteria is chosen such that under most circumstances it will not be triggered.

If the DS2181 is used with a processor, then the user may choose his own threshold by using the on-chip CRC4 Error Count Register (CECR) that can be only one possible CRC4 word error in 1 ms, the counter can be used to monitor errors for a 255 ms period before saturation. This period can be extended by reading the CECR every 200 ms, clearing it, and accumulating the error count in a host microcontroller. The result is with five "reads," a one second monitoring period can be established.

For example, a threshold of 915 CRC4 word errors in a one second monitoring periiod can be set this way. The re-sync process can be manually initiated using bit position 0 in the Receive Control Register (RCR.0).

For hardware mode applications of the DS2181, the RFER pin may be used with RCSYNC pin to demultiplex the CRC4 word errors. Errors are then counted externally. The re-sync process can be manually initiated using the Reset pin.

CAS SIGNALLING SOURCE

CAS applications sample signalling data at TSER when TCR.6 = 0; an on-chip data multiplexer accepts "channel associated" data input at TSD when TCR.6 = 1. The data multiplexer must be disabled (TCR.6 = 0) when the CCS mode is enabled (TCR.5 = 1).

TSD INPUT TIMING (TCR.6 = 1; TCR.5 = 0) Table 6

Frame #	Timeslot signalling data sampled at TSD
0	17
1	1,18
2	2,19
3	3,20
4	4,21
5	5,22
6	6,23
7	7,24
8	8,25
9	9,26
10	10,27
11	11,28
12	12,29
13	13,30
14	14,31
15	15

NOTES:
1. A, B, C and D data is sampled on falling edges of TCLK during bit times 5, 6, 7 and 8 of timeslots indicated.

TSD IPUT TIMING Figure 7
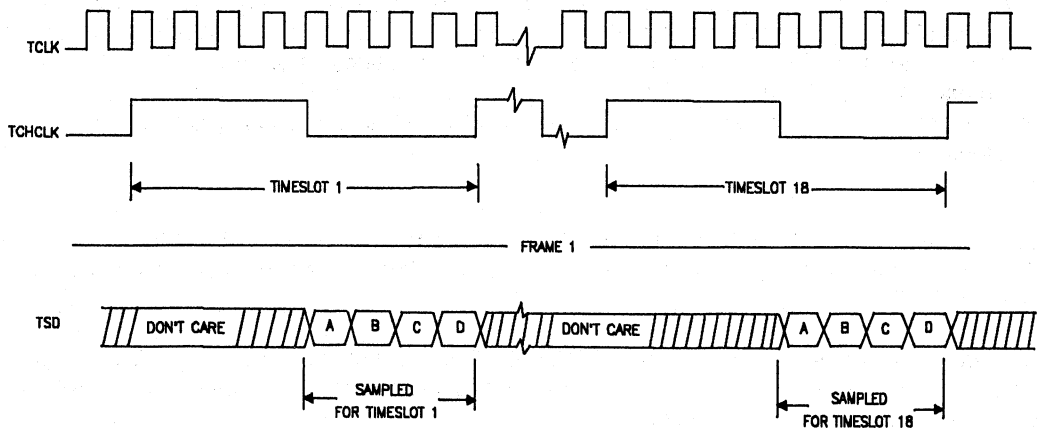
CAS OUTPUT FORMAT IN TIMESLOT 16 Figure 8

Frame 0[1]	Frame 1		- - -	Frame 15	
0000 XYXX	ABCD for timeslot 1	ABCD for timeslot 17	- - -	ABCD for timeslot 15	ABCD for timeslot 31

NOTES:
1. Timeslot 16 of frame 0 is reserved for the multiframe alignment word (0000), distant multiframe alarm (Y) and extra bits (X-XX).

TINR: TRANSMIT INTERNATIONAL AND NATIONAL REGISTER Figure 9

(MSB)   (LSB)

INB	- -	TRA	NB4	NB5	NB6	NB7	NB8

SYMBOL	POSITION	NAME AND DESCRIPTION
INB	TINR.7	**International Bit.** Inserted into the outgoing data stream when TCR.4 = 1.
- -	TINR.6	Reserved, must be 0 for proper operation.
TRA	TINR.5	**Transmit Remote Alarm** 0 = Normal operation; bit 3 of timeslot 0 in non-alignment frames clear. 1 = Alarm condition; bit 3 of timeslot 0 in non-align frames set.
NB4 NB5 NB6 NB7 NB8	TINR.4 TINR.3 TINR.2 TINR.1 TINR.0	**Transmit National Bits.** Inserted into the outgoing data stream at TPOS and TNEG when TCR.3 =

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TRANSMIT INTERNATIONAL AND NATIONAL DATA

Bit 1 of timeslot 0 in all frames in known as the international bit. When TCR.4 = 1, the transmitted international bit is sourced from TINR.7. When TCR.4 = 0, the transmitted international bit is sampled at TIND during the first bit period of each frame. The international bit positions in all outgoing frames except 13 and 15 are replaced by CRC4 codewords and the CRC4 multiframe alignment signal when CCR.3 = 1.

Bits 4 thru 8 of timeslot 0 in non-align frames are reserved for national use. When TCR.3 = 1, the transmitted national bits are sourced from registers locations TINR.4 thru TINR.0. If TCR.3 = 0, the national bits are sampled at TIND during bit times 4 thru 8 of timeslot 0 in non-align frames.

Reserved bit positions in the TINR must be set to 0 when written; those bits may be 0 or 1 when read.

TXR: TRANSMIT EXTRA REGISTER Figure 10

(MSB)   (LSB)

| - - | - - | - - | - - | XB1 | TDMA | XB2 | XB3 |

SYMBOL	POSITION	NAME AND DESCRIPTION
- -	TXR.7	Reserved, must be 0 for proper operation
- -	TXR.6	Reserved, must be 0 for proper operation
- -	TXR.5	Reserved, must be 0 for proper operation
- -	TXR.4	Reserved, must be 0 for proper operation
XB1	TXR.3	**Extra Bit 1**
TDMA	TXR.2	**Transmit Distant Multiframe Alarm** 0 = Normal operation; bit 6 of timeslot 16 in frame 0 clear 1 = Alarm condition; bit 6 of timeslot 16 in frame 0 set
XB2	TXR.1	**Extra Bit 2**
XB3	TXR.0	**Extra Bit 3**

TRANSMIT EXTRA DATA

In the CAS mode, timeslot 16 of frame 0 contains the multiframe alignment pattern, extra bits and the distant multiframe alarm. When CAS is enabled (TCR.5 = 0), the extra bits are sourced from TXR.0, TXR.1 and TXR.3 (TCR.2 = 1) or the extra bits are sampled externally at TXD during the extra bit time (TCR.2 = 0). The extra bits, alignment pattern and alarm signal are not utilized in the CCS mode (TCR.5 = 1), input TSER "overwrites" all timeslot 16 bit positions.

Reserved bit positions in the TXR must be set to 0 when written, those bits may be 0 or 1 when read.

TIR1 - TIR4: TRANSMIT IDLE REGISTERS Figure 11

(MSB)   (LSB)

TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0'	TIR1
TS15	TS14	TS13	TS12	TS11	TS10	TS9	TS8	TIR2
TS23	TS22	TS21	TS20	TS19	TS18	TS17	TS16'	TIR3
TS31	TS30	TS29	TS28	TS27	TS26	TS25	TS24	TIR4

SYMBOL POSITION   **NAME AND DESCRIPTION**

TS31   TIR4.7   **Transmit Idle Registers.** Each of these bit positions represent
TSO   TIR1.0   a timeslot in the outgoing stream at TPOS and TNEG; when set the
                         contents of that timeslot are forced to idle code (11010101).

NOTE: TS0 and TS16 are not affected by the idle register.

TRANSMIT TIMING

A low-high transition at TMSYNC once per multiframe (every 2 milliseconds) or at a multiple of the multiframe rate establishes outgoing CAS and/or CRC4 multiframe alignment. Output TMO indicates that alignment. A low-high transition at TFSYNC at the frame rate (125 us.) or at a multiple of the frame rate establishes the outgoing frame position. Output TAF indicates that alignment.

TMSYNC and/or TFSYNC may be tied low by the user, in which case the arbitrary frame and multiframe alignment established by the device will be indicated at TMO and TAF.

Output TAF also indicates frames containing the frame alignment signal. Those frames may be "even or odd" numbering frames of the outgoing CAS multiframe (CCR.6).

TRANSMIT MULTIFRAME TIMING Figure 12
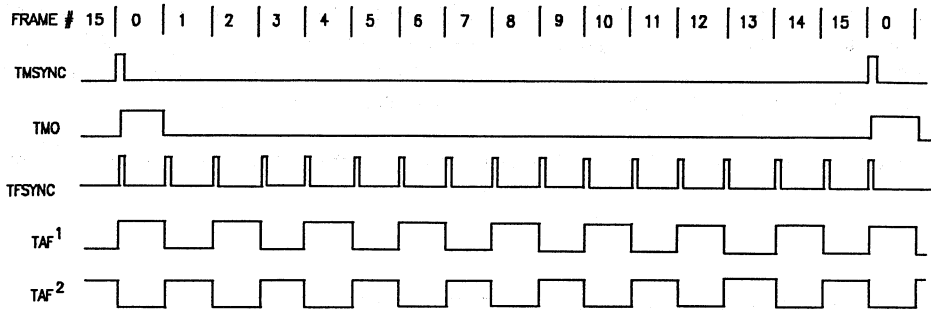
NOTES:
1. Alignment frames are "even" frames of the CAS and/or CRC4 multiframes (CCR.6 = 0).
2. Alignment frames are "odd" frames of the CAS multiframe (CCR.6 = 1).

TRANSMIT MULTIFRAME BOUNDARY TIMING Figure 13
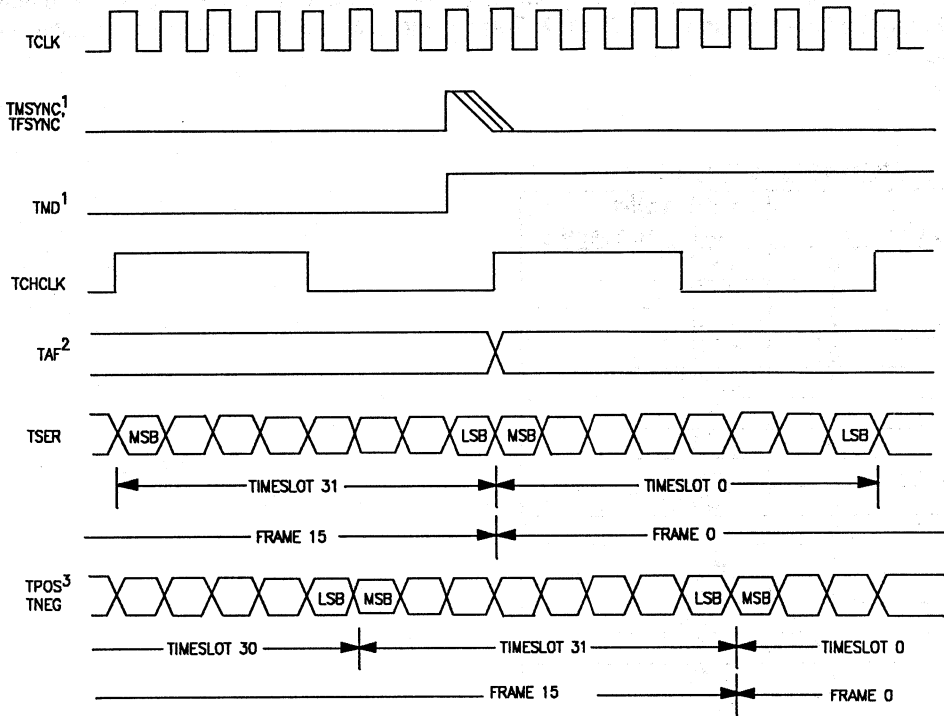
NOTES:
1. Low-high transitions on TMSYNC and/or TFSYNC must occur one TLCK period early with respect to actual frame and multiframe boundries. TMO follows the rising edge of TMSYNC or TFSYNC.
2. TAF transitions on true frame boundries.
3. Delay from TSER to TPOS, TNEG is five TCLK periods.

TRANSMIT SIGNALING TIMESLOT TIMING Figure 14
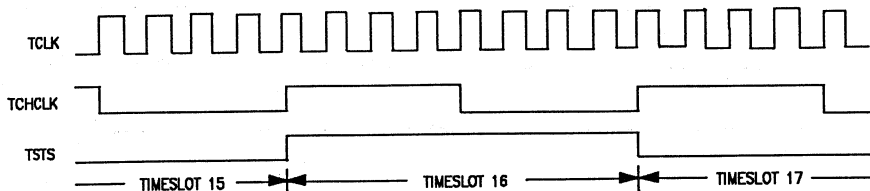
RECEIVE SIGNALING

Receive signalling data is available at two outputs; RSER and RSD. RSER outputs the signalling data in timeslot 16 at RSER. The signalling data is also extracted from timeslot 16 and presented at RSD during the timeslots shown in Table 7. This "channel associated" signalling simplifies CAS system design.

RECEIVE SIGNALING Table 7

Frame #	RSD[1] valid during timeslot #
0	15,[2]
1	[2],17
2	1,18
3	2,19
4	3,20
5	4,21
6	5,22
7	6,23
8	7,24
9	8,25
10	9,26
11	10,27
12	11,28
13	12,29
14	13,30
15	4,31

NOTES: applicable only to CAS systems
1. RSD is valid for the least significant nibble in each indicated timeslot. Timeslot A data appears in bit 5, B in bit 6, C in bit 7 and D in bit 8.
2. RSD does not output valid data during timeslots 0 and 16.

RSD TIMING Figure 15
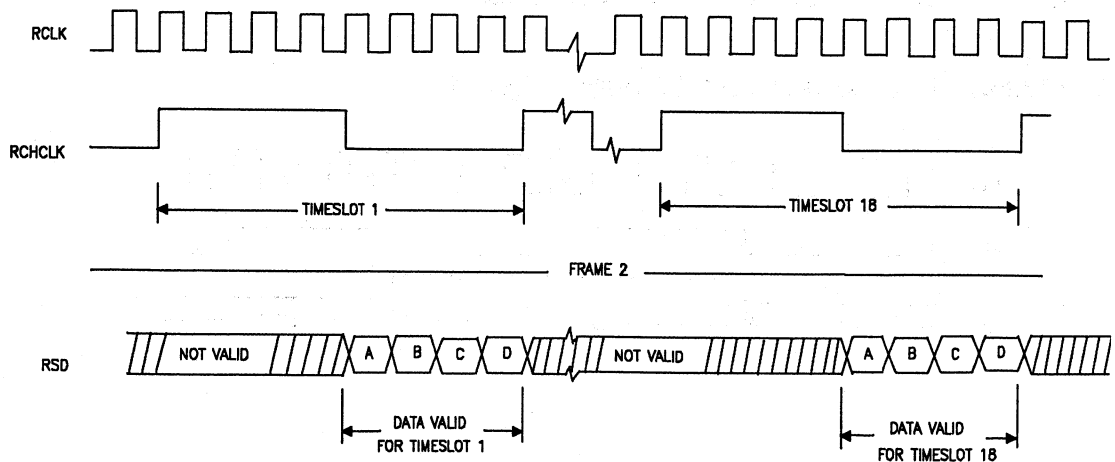
RECEIVE TIMING

The receive side output timing set is identical to that found on the tranmit side. The user may tie receive outputs directly to the transmit inputs for "drop and insert" applications. The received data of RPOS, RNEG appear at RSER after six RCLK delays, without any change except for the HDB3 to NRZ conversion when HDB3 is enabled.

RECEIVE MULTIFRAME TIMING Figure 16
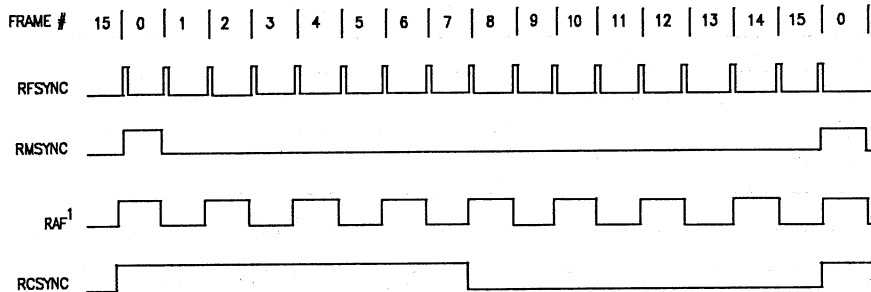
NOTES:

1. The CAS multiframe may start with an align or non-align frame. The CRC4 multiframe always starts with an align frame.

RECEIVE MULTIFRAME BOUNDARY TIMING Figure 17
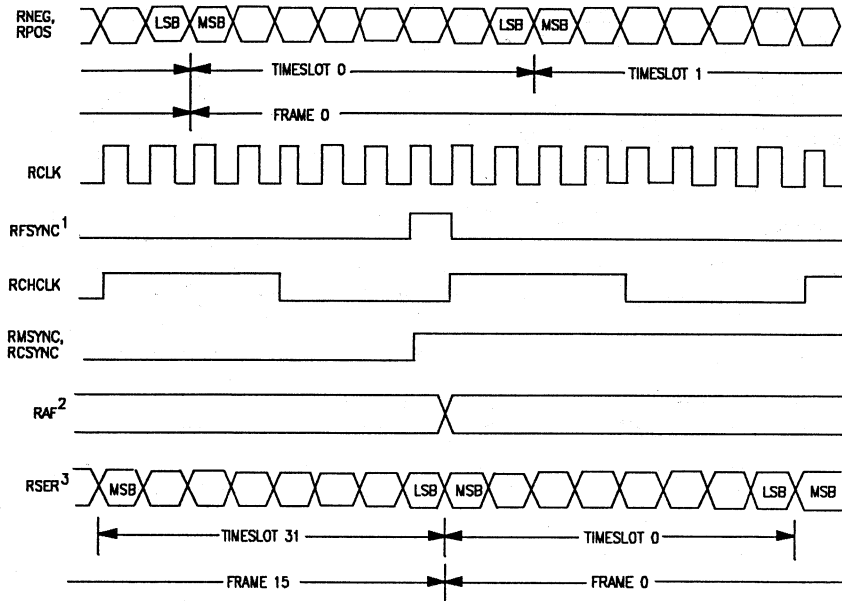
**NOTES:**
1. Low-high transitions on RMSYNC and RFSYNC occur one RCLK period early with respect to actual frame and multiframe boundries.
2. RAF transitions on true frame boundries.
3. Delay from RPOS, RNEG to RSER is six RCLK periods.

RSR: RECEIVE STATUS REGISTER Figure 18

(MSB)   (LSB)

| RRA | RDMA | RSA1 | RUA1 | FSERR | MFSERR | RLOS | ECS |

SYMBOL	POSITION	NAME AND DESCRIPTION
RRA	RSR.7	**Receive Remote Alarm.** Set when bit 3 of timeslot 0 in non-align frames set for three consecutive non-align frames.
RDMA	RSR.6	**Receive Distant Multiframe Alarm.** Set when bit 6 of timeslot 16 in frame 0 set for three consecutive multiframes.
RSA1	RSR.5	**Receive Signalling All "1s."** Set when contents of timeslot 16 have been all "1s" for two consecutive frames.
RUA1	RSR.4	**Receive Unframed All "1s."** Set when < 3 bit positions of the last align and non-align frames received have been 0.
FSERR	RSR.3	**Frame Resync Criteria Met.** Set when the Frame Error Criteria is met, also the Frame Resync is initiated if RCR.1 = 0.
MFSERR	RSR.2	**CAS Multiframe Resync Criteria Met.** Set when the CAS multiframe error criteria is met, also the Frame Resync is initiated if RCR.1 = 0.
RLOS	RSR.1	**Receive Loss of Sync.** Set when resync is in progress.
ECS	RSR.0	**Error Count Saturation.** Set when any of the on-chip counters at FECR, CECR or BVCR saturates.

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NOTES:
1. When in the CCS mode, the RDMA flag bit and the RDMA pin have no significance. It will be set when bit 6 of Timeslot 16 in Frame 0 is set for three consecutive multiframes in either CAS or CCS mode.

RIMR: RECEIVE INTERRUPT MASK REGISTER Figure 19

(MSB)   (LSB)

| RRA | RDMA | RSA1 | RUA1 | FSERR | MFSERR | RLOS | ECS |

SYMBOL	POSITION	NAME AND DESCRIPTION
RRA	RIMR.7	**Receive Remote Alarm** I = Interrupt enabled O = Interrupt masked
RDMA	RIMR.6	**Receive Distant Multiframe Alarm.** I = Interrupt enabled O = Interrupt masked
RSA1	RIMR.5	**Receive Signalling All "1s."** I = Interrupt enabled O = Interrupt masked
RUA1	RIMR.4	**Receive Unframed All "1s."** I = Interrupt enabled O = Interrupt masked
FSERR	RIMR.3	**Frame Resync Criteria Met.** I = Interrupt enabled O = Interrupt masked
MFSERR	RIMR.2	**CAS Multiframe Resync Criteria Met.** I = Interrupt enabled O = Interrupt masked
RLOS	RIMR.1	**Receive Loss of Sync.** I = Interrupt enabled O = Interrupt masked
ECS	RIMR.0	**Error Count Saturation.** I = Interrupt enabled O = Interrupt masked

ALARM REPORTING AND INTERRUPT SERVICING

Alarm and error conditions are reported at outputs and the RSR. Use of the RSR and error count registers simplifies system error monitoring. The RSR may be read in one of two ways: a burst read does not disturb the RSR contents, a direct read will clear all bits set in the RSR unless the alarm condition which set them is still active.

Interrupts are enabled via the RIMR and are generated whenever an alarm or error condition sets an RSR bit. The host controller must service the tranceiver in order to clear an interrupt condition. Clearing the appropriate RIMR bit will unconditionally clear an interrupt.

BVCR: BIPOLAR VIOLATION COUNT REGISTER Figure 20

(MSB)							(LSB)
BVD7	BVD6	BVD5	BVD4	BVD3	BVD2	BVD1	BVD0

SYMBOL	POSITION	NAME AND DESCRIPTION
BVD7	BVCR.7	MSB of bipolar violation count.
BVD0	BVCR.0	LSB of bipolar violation count.

CECR: CRC4 ERROR COUNT REGISTER Figure 21

(MSB)							(LSB)
CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0

SYMBOL	POSITION	NAME AND DESCRIPTION
CRC7	BVCR.7	MSB of CRC4 Error Count.
CRC0	BVCR.0	LSB of CRC4 Error Count.

FECR: FRAME ERROR COUNT REGISTER Figure 22

(MSB)							(LSB)
FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0

SYMBOL	POSITION	NAME AND DESCRIPTION
FE7	FECR.7	MSB of frame error count.
FE0	FECR.0	LSB of frame error count.

ERROR LOGGING

The BVCR, CECR and FECR contain eight bit binary up counters which increment on individual bipolar violations, CRC4 code word errors (when CCR.2 = 1), and word errors in the frame alignment signal. Each counter saturates at 255. Once saturated, each following error occurance will generate an interrupt (RIMR.0 = 1) until the register is reporgrammed to a value other than FF (hex). Presetting the registers allows the user to establish specific error count thresholds; the counter will count "up" to saturation from the preset value. The BVCR increments at all times (regardless of sync status). CECR and FECR increments are disabled whenever resync is in progress (RLOS high).

ALARM OUTPUTS

Alarm conditions are also reported real time at alarm outputs. These outputs may be used with off-chip logic to complement the on-chip error reporting capability of the DS2181. In the hardware mode, they are the only alarm reporting means available.

RLOS

The RLOS output indicates the status of the receive synchronizer. When high, frame, CAS multiframe and/or CRC4 multiframe synchronization is in progress. A high-low transition indicates resync is complete. The RLOS bit (RSR.1) is a "latched" version of the RLOS output.

RRA

The remote alarm output transitions high when a remote alarm is detected. A high-low transition indicates the alarm condition has been cleared. The alarm condition is defined as bit 3 of timeslot 0 set for three consecutive non-align frames. The alarm state is cleared when bit 3 has been clear for three consecutive non-align frames. The RRA bit (RSR.7) is a "latched" version of the RRA output.

RBV

RBV outputs one RCLK pulse when the accused bit emerges at RSER. RBV will return low when RCLK goes low, and RBV pin Bipolar violations are logged in the BVCR. The RBV pin provides a pulse for every violation which can be counted externally.

RDMA

RDMA transitions high when bit 6 of timeslot 16 in frame 0 is set for three consecutive occasions and returns low when the bit is clear for three consecutive occasions. The RDMA bit (RSR.6) is a "latched" version of the RDMA output.

RCL

Transitions high after 32 consecutive "0s" appear at RPOS and RNEG, goes low at next 1 occurance.

RFER

The RFER output transitions high when received frame alignment, CAS multiframe alignment and/ or CRC4 code words are in error. The FECR and CECR log error events reported at this output. FECR logs only the Frame Alignment errors. CECR logs CRC4 code word errors.

To complement the on-chip error logging capabilities of the DS2181, the system designer may use off-chip logic gated by receive side outputs RCHCLK, RAF, RSTS and RCSYNC to demux error states present at RFER.

RFER OUTPUT TIMING FOR ALL ERROR CONDITIONS Figure 23

RFSYNC

RAF

RNSYNC

RCSYNC

RFER
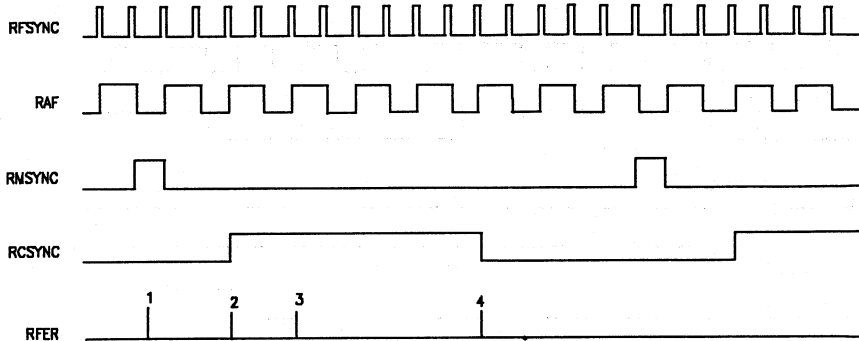
CAS MULTIFRAME ALIGNMENT ERROR Figure 24

RCLK

RCHCLK

RSTS

RFER [1]
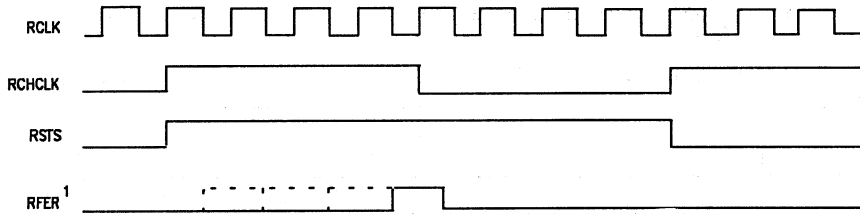
CRC4 SUB-MULTIFRAME 2 ERRORED Figure 25

RCLK

RCHCLK

RFSYNC

RAF

RCSYNC

RFER [2]
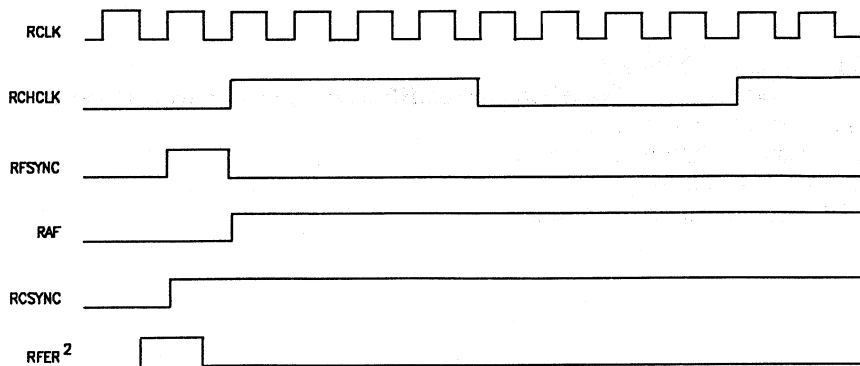
FRAME ALIGNMENT WORD ERRORED Figure 26
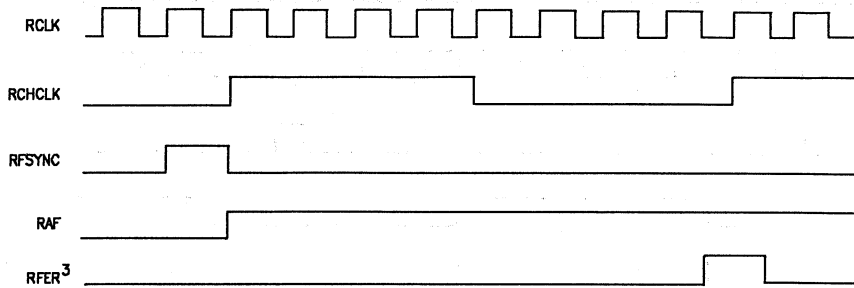
CRC4 SUB-MULTIFRAME 1 ERRORED Figure 27
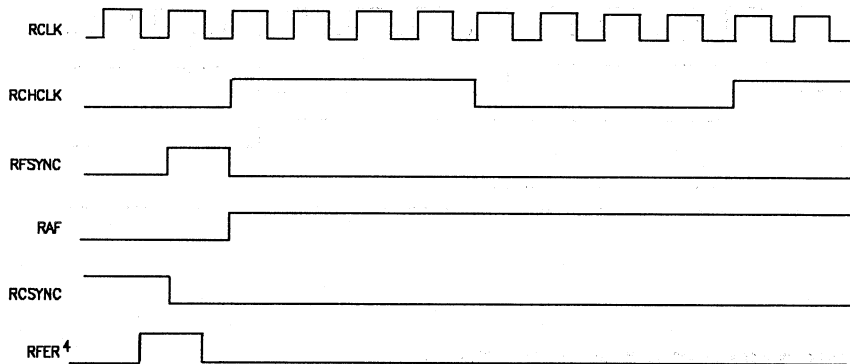
NOTES FOR FIGURES 23 THRU 27:
1. CAS multiframe alignment word received in error, RFER will transition high at first error occurance and remain high as shown.
2. Previous CRC4 sub-multiframe 2 errored.
3. Frame alignment word errored.
4. Previous CRC4 sub-multiframe 1 errored.

RESET
A high-low transition on RST clears all internal registers except the three error counters; a resync is initiated until RST returns high. RST must be held low on system power-up and when switching to/from the hardware mode. Following reset, the host processor should update all on-chip registers to establish desired operating modes.

HARDWARE MODE
An on-chip hardware control mode simplifies preliminary system prototyping and serves applications which do not require the features of the serial port. Tying SPS low disables the serial port, clears all internal registers locations except those shown below and redefines pins 14 thru 18 as mode control inputs. The mode control inputs establish device operational characteristics as shown in Table 8. The hardware mode simplifies device retrofit into existing applications where control interfaces are designed with discrete logic.

HARDWARE MODE CONTROL Table 8

PIN NUMBER	REGISTER LOCATION	NAME AND DESCRIPTION
14	TINR.5	**TRA - Transmit Remote Alarm** 0 = Normal operation 1 = Enable alarm
15	TXR.2	**TDMA - Transmit Distant Multiframe Alarm** 0 = Normal operation 1 = Enable alarm
16	CCR.5/ CCR.4	**Data Format** 0 = Input and output data AMI coded 1 = Input and output data HDB3 coded
17	CCR.3/ CCR.2	**Transmit and Receive CRC4 Multiframe** 0 = Disabled 1 = Enabled
18	TCR.3/ RCR.2	**Transmit and Receive CAS Multiframe** 0 = Enabled 1 = Disabled

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ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-	-1.0V to +7V
OPERATING TEMPERATURE	-	0° to 70° C
STORAGE TEMPERATURE	-	-55° to +125° C
SOLDERING TEMPERATURE	-	260° C for 10 sec.

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS   (0 to 70 deg. C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Logic 1	V_{IH}	2.0		V_{DD}+.3	V
Logic 0	V_{IL}	-0.3		+0.8	V
Supply	V_{DD}	4.5		5.5	V

D.C. ELECTRICAL CHARACTERISTICS   (0 to 70 deg. C V_{DD}=5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		6		mA	1,2
Input Leakage	I_{IL}	-1.0		+1.0	uA	3
Output Current @ 2.4V	I_{OH}	-1.0			mA	4
Output Current @ 0.4V	I_{OL}	+4.0			mA	5
Output Leakage	I_{LO}	-1.0		+1.0	uA	6

Notes:
1. TCLK = RCLK = 2.048 MHz
2. Outputs open
3. 0V < V_{IN} < V_{DD}
4. All outputs except INT which is open collector
5. All outputs
6. Applies to SDO when tristated

CAPACITANCE ($t_A = 25^oC$)

PARAMETER	SYMBOL		MAX	UNITS
Input Capacitance	C_{IN}		5	pF
Output Capacitance	C_{OUT}		7	pF

A.C. ELECTRICAL CHARACTERISTICS[1,2] SERIAL PORT

(0 to 70 deg. C, $V_{DD} = 5V \pm 5\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SDI to SCLK Setup	t_{DC}	50			ns
SCLK to SDI Hold	t_{CDH}	50			ns
SDI to SCLK Falling edge	t_{CD}	50			ns
SCLK low time	t_{CL}	244			ns
SCLK high time	t_{CH}	244			ns
SCLK Rise and Fall times	t_R, t_F			100	ns
CS to SCLK Setup	t_{CC}	50			ns
SCLK to CS hold	t_{CCH}	50			ns
CS Inactive time	t_{CWH}	2.5			us
SCLK to SDO Valid	t_{CDV}			200	ns
CS to SDO High Z	t_{CDZ}			75	ns

NOTES:

1. Measured at $V_{IH} = 2.0$ or $V_{IL} = .8$ and 10 ns maximum rise and fall time.
2. Output load capacitance = 100 pf.

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SERIAL PORT WRITE A.C. TIMING DIAGRAM Figure 28
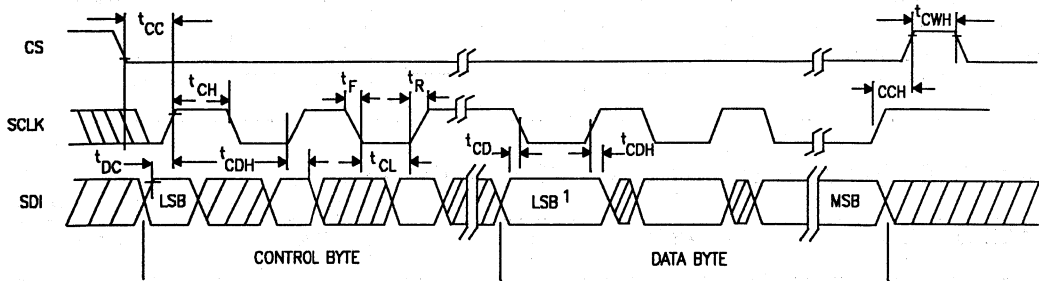
NOTES:
1. Data byte bits must be valid across low clock periods to prevent transients in operating modes.
2. Shaded regions indicate "don't care" states of input data.

SERIAL PORT READ[1] A.C. TIMING Figure 29
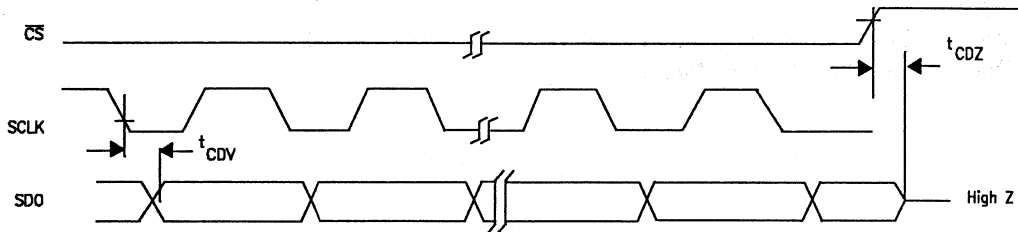
NOTES:
1. Serial port write must precede a port read to provide address information.

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A.C. ELECTRICAL CHARACTERISTICS[1,2] TRANSMIT (0 to 70 deg. C, VDD = 5V ±5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
TCLK period	t_p		488		ns
TCLK pulse width	t_{WL}, t_{WH}		244		ns
TCLK Rise and Fall times	t_R, t_F		20		ns
TSER, TSD, TIND and TXD Setup to TCLK fallling	t_{STD}	50			ns
TSER, TSD, TIND and TXD Hold to TCLK falling	t_{HTD}	50			ns
TFSYNC, TMSYNC Setup to TCLK falling	t_{STS}	75			ns
TFSYNC, TMSYNC Hold to TCLK falling	t_{HTS}	50			ns
Propagation Delay TCLK to TCHCLK, TSTS, TMO, TAF	t_{PTS}			75	ns

NOTES:
1. Measured at V_{IH} = 2.0 or V_{IL} = .8 and 10 ns maximum rise and fall time.
2. Output load capacitance = 100 pf.

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TRANSMIT A.C. TIMING DIAGRAM Figure 30
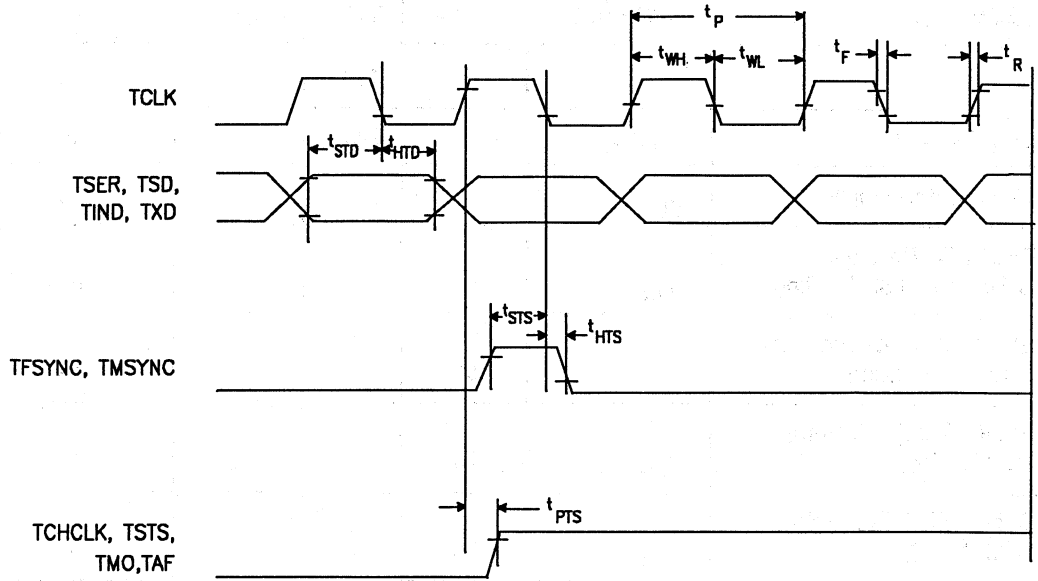
A.C. ELECTRICAL CHARACTERISTICS[1,2] RECEIVE (0 to 70 deg. C, VDD = 5V ±5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Propagation Delay RCLK to RMSYNC, RFSYNC, RSTS, RCHCLK, RAF	t_{PRS}			75	ns
Propagation Delay RCLK to RSER, RSD	t_{PRD}			75	ns
Transition time all outputs	t_{TTR}			20	ns
RCLK period	t_P		488		ns
RCLK pulse width	t_{WL}, t_{WH}		244		ns
RCLK rise and fall times	t_R, t_F		20		ns
RPOS, RNEG Set Up to RCLK Falling	t_{SRD}	50			ns
RPOS, RNEG Hold to RCLK Falling	t_{HRD}	50			ns
Propagation Delay RCLK to RLOS, RRA, RBV, RFER, RDMA, RCL	t_{PRA}			75	ns
Minimum RST Pulse Width	t_{RST}	1			us

NOTES:
1. Measured at V_{IH} = 2.0 or V_{IL} = .8 and 10 ns. maximum rise anf fall time.
2. Output load capacitance = 100 pf.

5

RECEIVE A.C. TIMING DIAGRAM Figure 31
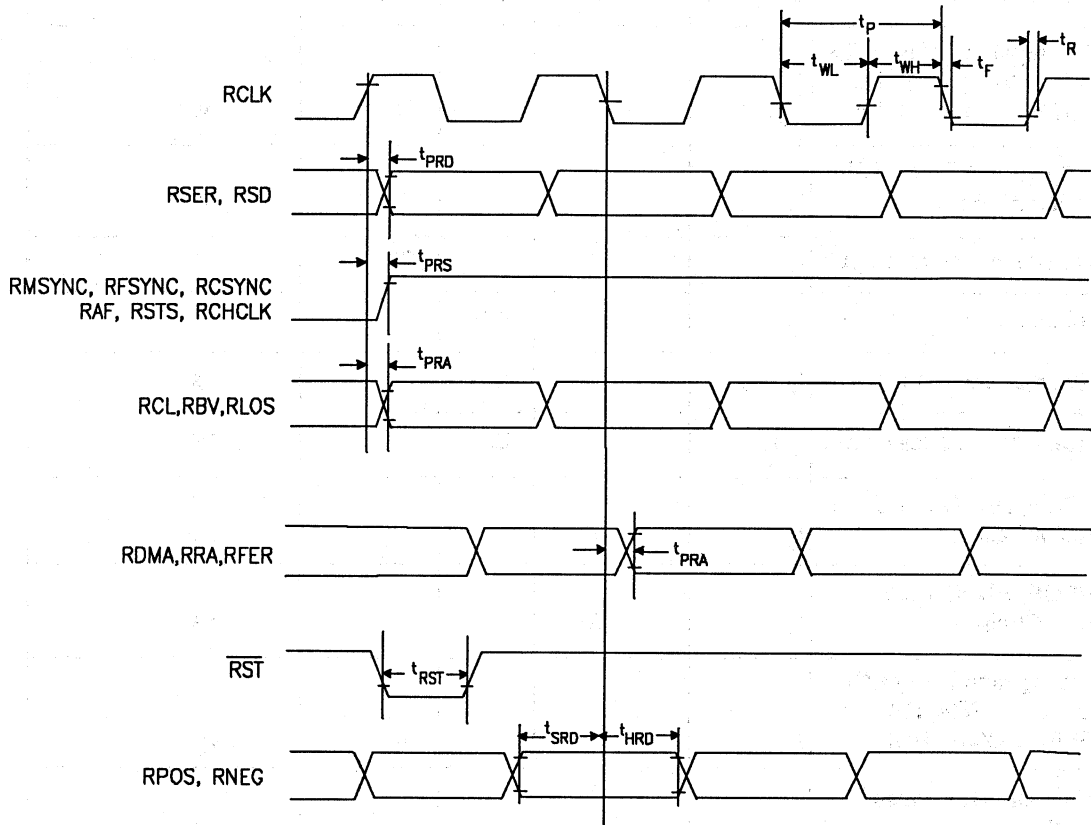
DS2181
Serial CEPT Transceiver
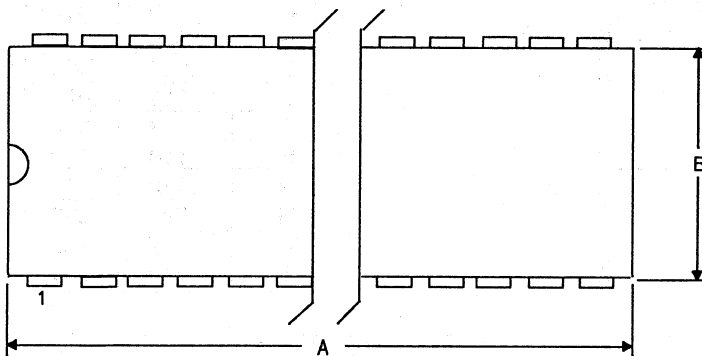
DIM.	INCHES	
	MIN.	MAX.
A	2.040	2.080
B	.540	.560
C	.140	.160
D	.590	.610
E	.020	.040
F	.110	.130
G	.090	.110
H	.600	.680
J	.008	.012
K	.015	.021

19 EQUAL SPACES AT
100 + .010 TNA
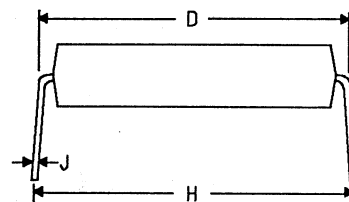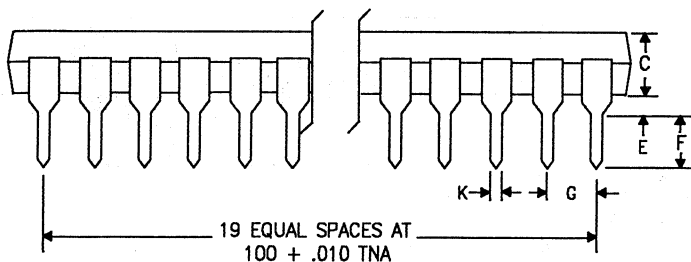
5

DS2181Q
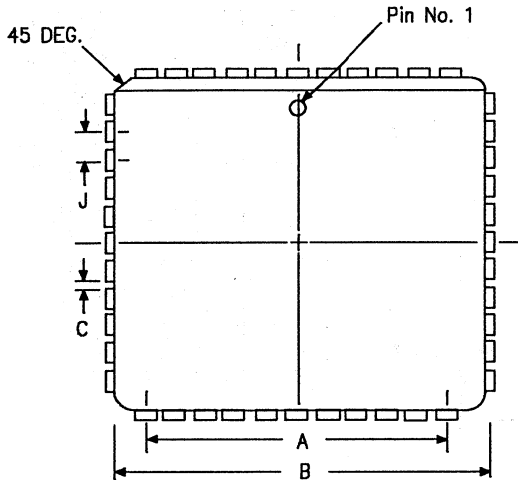
DIM.	INCHES	
	MIN.	MAX.
A	.490	.510
B	.590	.630
C	.020	.024
D	.018	.022
E	.688	.692
F	.118	.122
G	.020	.030
H	.590	.630
I	.167	.173
J	.048	.051

Line Interfaces

Dallas Semiconductor
Transmit Line Interface
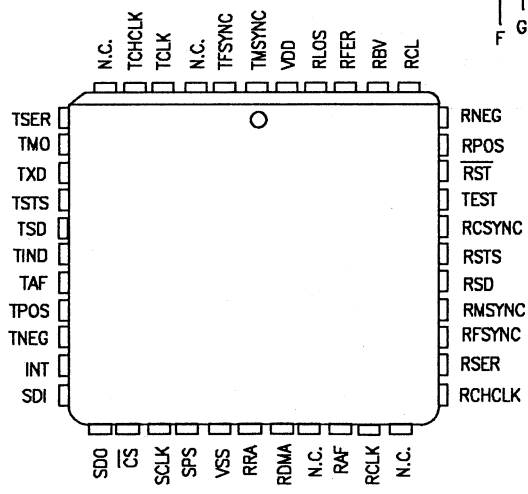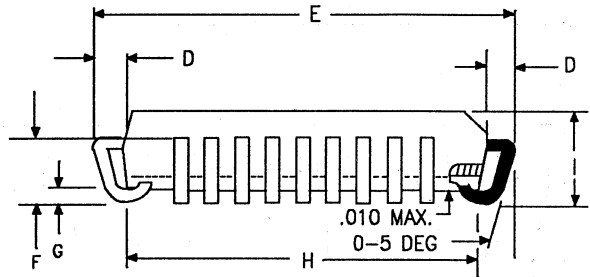
FEATURES

● Line interface for T1 (1.544 MHz) and CEPT (2.048 MHz) primary rate networks

● On-chip Transmit LBO (line build-out) and line drivers eliminate external components

● Programmable output pulse shape supports short and long loop applications

● Supports bipolar and unipolar input data formats

● Transparent, B8ZS and HDB3 zero code suppression modes

● Compatible with DS2180A T1 and DS2181 CEPT Transceivers

● Companion to the DS2187 and DS2189 Receive Line Interface

● Single 5V supply, low power CMOS technology

PIN CONNECTIONS

TAIS	1	20	LCLK
ZCSEN	2	19	LPOS
TCLKSEL	3	18	LNEG
LEN0	4	17	TCLK
LEN1	5	16	TPOS
LEN2	6	15	TNEG
VDD	7	14	LB
TTIP	8	13	MTIP
TRING	9	12	MRING
VSS	10	11	$\overline{LF}$

DESCRIPTION

The DS2186 interfaces user equipment to North American (T1-1.544 MHz) and European (CEPT-2.048 MHz) primary rate communications networks. The device is compatible with all types of twisted pair and coax cable found in such networks.

Key on-chip components include: programmable waveshaping circuitry, line drivers, remote loopback and zero suppression logic. A line-coupling transformer is the only external component required.
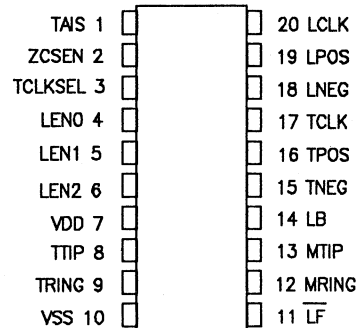
Short loop (DSX-1, 0 to 655 feet) and long loop (CSU; 0 db, -7.5 db and -15 db) pulse templates found in T1 applications are supported. Appropriate CCITT Red Book recommendations are met in the CEPT mode.

Application areas include DACS, CSU, CPE, channel banks and PABX to computer interfaces such as DMI and CPI. Supports ISDN -PRI (primary rate interface) specifications.

DS2186 BLOCK DIAGRAM Figure 1
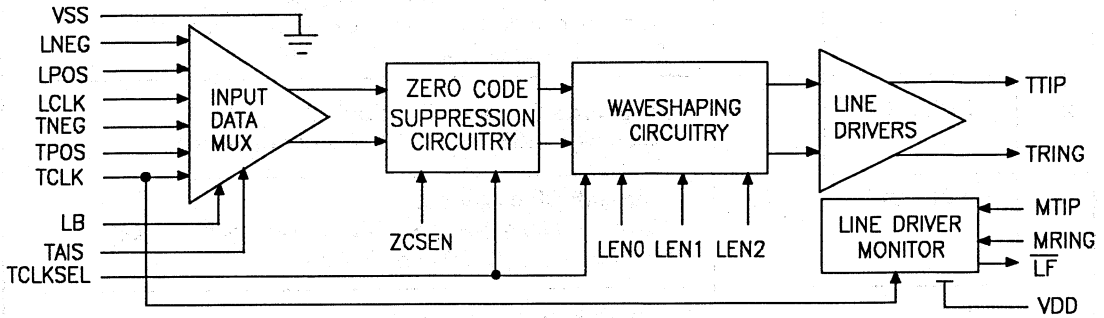
SYSTEM LEVEL INTERCONNECT Figure 2
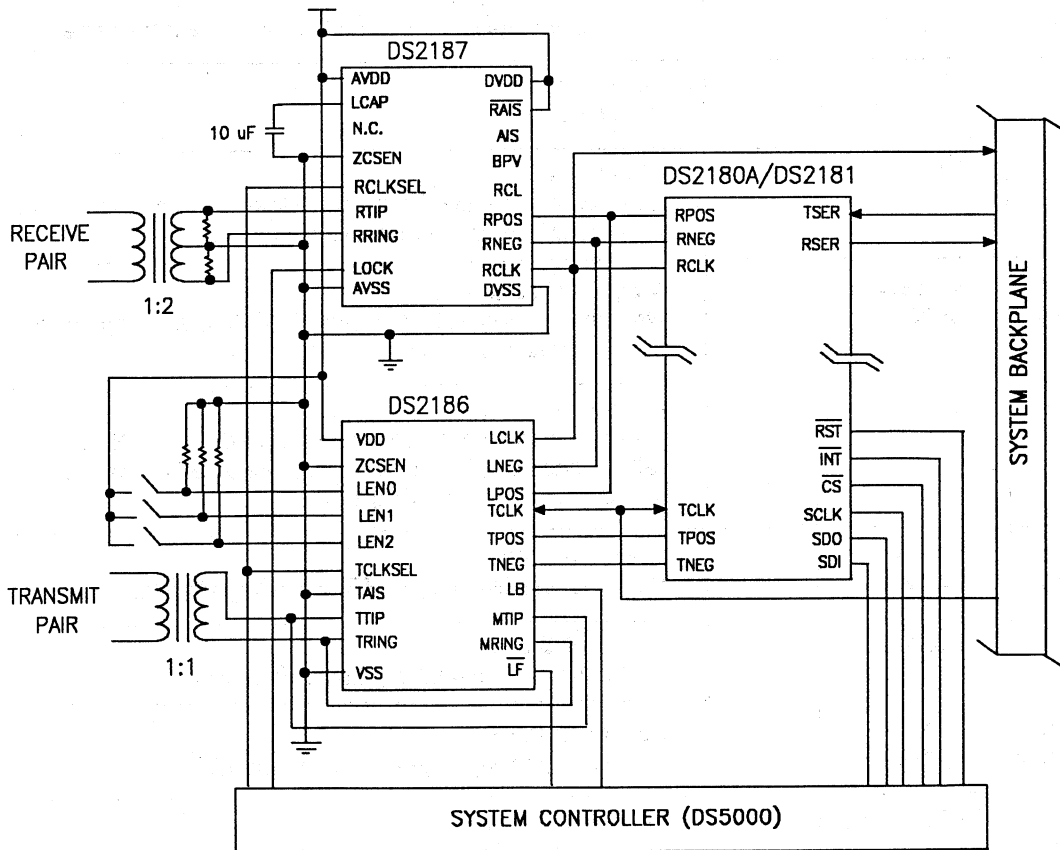
PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	TAIS	I	**Transmit Alarm Indication Signal** When high, output data is forced to all "ones" at the TCLK (LB = 0) or LCLK (LB = 1) rate.
2	ZCSEN	I	**Zero Code Suppression Enable** When high, B8ZS or HDB3 encoder enabled.
3	TCLKSEL	I	**Transmit Clock Select** Tie to VSS for 1.544 MHz (T1) applications, to VDD for 2.048 MHz (CEPT) applications.
4 5 6	LEN0 LEN1 LEN2	I	**Length Select 0, 1 and 2** State determines output T1 waveform shape and characteristics.
7	VDD	- -	**Positive Supply** 5.0 volts.
8 9	TTIP, TRING	O	**Transmit Tip and Ring** Line driver outputs, connect to transmit line transformer
10	VSS	- -	**Signal Ground** 0.0 Volts.
11	$\overline{\text{LF}}$	O	**Line Fault** Open collector active low output. Held low during an output driver fault and/or failure; tristated otherwise.
12 13	MRING, MTIP	I	**Monitor Tip and Ring** Normally connected to TTIP and TRING. Sense inputs for line fault detection circuitry.
14	LB	I	**Loopback** When high, input data is sampled at LPOS and LNEG on falling edges of LCLK; when low, input data is sampled at TPOS and TNEG on falling TCLK.
15 16	TNEG, TPOS	I	**Transmit Data** Sampled on falling edges of TCLK when LB = 0.
17	TCLK	I	**Transmit Clock** 1.544 MHz or 2.048 MHz primary data clock.
18 19	LNEG, LPOS	I	**Loopback Data** Sampled on falling edges of LCLK when LB = 1.
20	LCLK	I	**Loopback Clock** 1.544 MHz or 2.048 MHz loopback data clock.

INPUT DATA MODES
Input data is sampled on the falling edge of TCLK or LCLK and may be bipolar (dual rail) or unipolar (single rail, NRZ). TPOS, TNEG and TCLK are the data and clock inputs when LB = 0; LPOS, LNEG and LCLK when LB = 1. TPOS and TNEG (LPOS and LNEG) must be tied together in NRZ applications.

ZERO CODE SUPPRESSION MODES
Transmitted data is treated transparently (no zero code supression) when ZCSEN = 0. HDB3 code words replace any all-zero nibble when ZCSEN = 1 and TCLKSEL = 1. B8ZS code words replace any incoming all-zero byte when ZCSEN = 1 and TCLKSEL = 0.

ALARM INDICATION SIGNAL
When TAIS is set the all "ones" code is continuously transmitted at the TCLK rate (LB = 0) or the LCLK rate (LB = 1).

WAVESHAPING
The device supports T1 short loop (DSX-1; 0 to 655 feet), T1 long loop (CSU; 0 db, -7.5 db and -15 db) and CEPT (CCITT Red Book G.703) pulse template requirements. On-chip laser trimmed delay lines clocked by either TCLK or LCLK control a precision digital-to-analog converter to build the desired waveforms which are buffered differentially by the line drivers.

The shape of the "pre-emphasized" T1 waveform is controlled by inputs LEN0, LEN1, and LEN2 (TCLKSEL = 0). These control inputs allow the user to select the appropriate output pulse shape to meet DSX-1 or CSU templates over a wide variety of cable types and lengths. Those cable types include: ABAM, PIC and PULP.

The CEPT mode is enabled when TCLKSEL = 1. Only one output pulse shape is available in the CEPT mode; inputs LEN0, LEN1 and LEN2 may be any state except all zeros.

The line coupling transformer also contributes to the pulse shape seen at the cross-connect point; using the transformers specified in Table 4 insures the measured waveform meets DSX-1 and/or CSU template requirements. Transformers are 1:1.

The waveshaping circuitry does not contribute significantly to output jitter. Output jitter will be dominated by the jitter on TCLK or LCLK. TCLK and LCLK need only be accurate in frequency, not duty cycle.

LINE DRIVERS
The on-chip differential line drivers interface directly to the output transformer. To optimize device performance, length of the TTIP and TRING traces should be minimized and isolated from neighboring interconnect. The device will enter a standby mode when the input data is all "zeros." This disables the output drivers and reduces power consumption significantly.

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FAULT PROTECTION

The line drivers are fault protected and will withstand a shorted transformer secondary (or primary) without damage. Inputs MTIP and MRING are normally tied to TTIP and TRING to provide fault monitoring capability. Output LF will transition low if 192 TCLK cycles occur without a "one" occuring at MTIP or MRING. LF will tristate on the next "one" occurance or two TCLK periods later, whichever is greater.

The "one" threshold of MTIP and MRING varies with the line type selected at LEN0, LEN1 and LEN2. This insures detection of the lowest level 0 to 1 transition (-15 dB buildout) as it occurs on TTIP and TRING. MTIP and MRING may be tied to neighboring device's TTIP and TRING outputs to provide superior fault monitoring.

T1 LINE LENGTH SELECTION Table 2

LEN2	LEN1	LEN0	OPTION SELECTED	APPLICATION
0	0	0	Test mode	Do not use
0	0	1	-7.5 dB buildout	T1 CSU
0	1	0	-15 dB buildout	T1 CSU
0	1	1	0 dB buildout, 0 - 133 feet	T1 CSU, DSX-1 Crossconnect
1	0	0	133 - 266 feet	DSX-1 Crossconnect
1	0	1	266 - 399 feet	DSX-1 Crossconnect
1	1	0	399 - 533 feet	DSX-1 Crossconnect
1	1	1	533 - 655 feet	DSX-1 Crossconnect

NOTE:
1. The LEN0, LEN1 and LEN2 inputs control T1 output waveshapes when TCLKSEL = 0. The G.703 (CEPT) template is selected when TCLKSEL = 1 and LEN0, LEN1 and LEN2 are at any state except all zeros.

DSX-1 ISOLATED PULSE TEMPLATE Figure 3
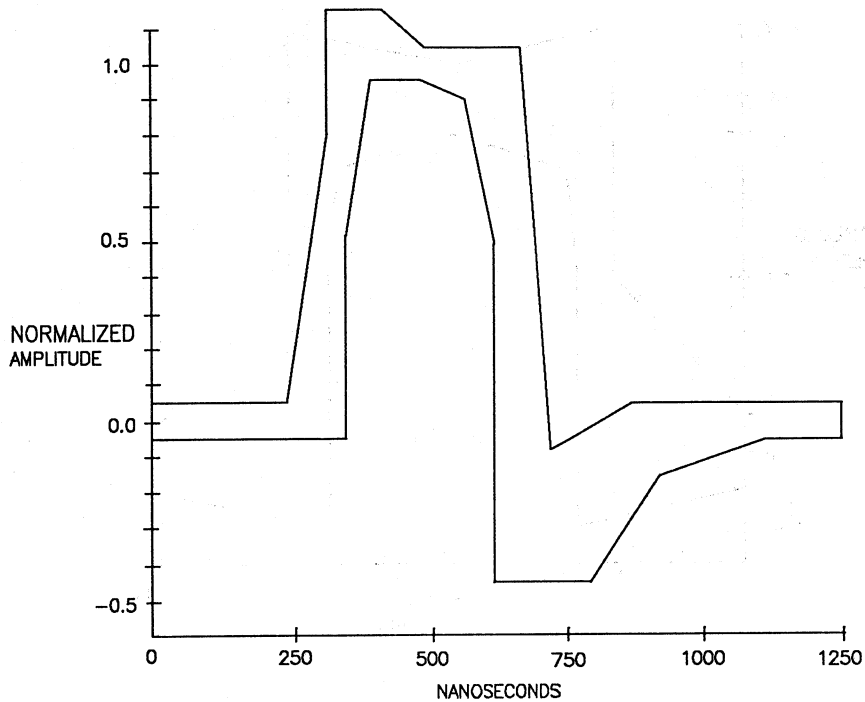
NOTES:
1. Template shown is measured at the cross-connect point.
2. Amplitude shown is normalized; the actual midpoint voltage measured may be between 2.4 and 3.6 volts.
3. The corner points shown below are joined by straight lines to form the template.

MAXIMUM CURVE	MINIMUM CURVE
(0, 0.05)	(0, -0.05)
(250, 0.05)	(350, -0.05)
(325, 0.80)	(350, 0.5)
(325, 1.15)	(400, 0.95)
(425, 1.15)	(500, 0.95)
(500, 1.05)	(600, 0.9)
(675, 1.05)	(650, 0.5)
(725, -0.07)	(650, -0.45)
(875, 0.05)	(800, -0.45)
(1250, 0.05)	(925, -0.2)
	(1100, -0.05)
	(1250, -0.05)

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OUTPUT PULSE TEMPLATE AT 2.048 MHz Figure 4
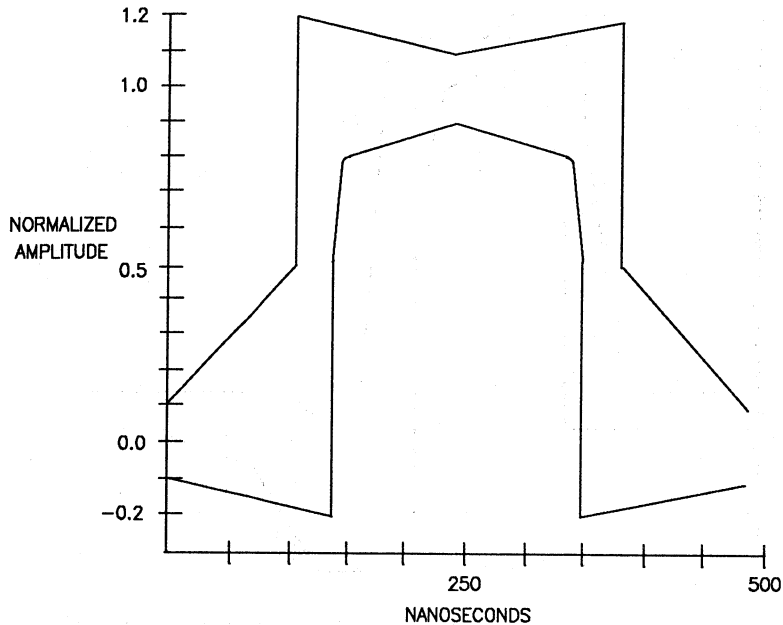
NOTES:
1. Unlike the DSX-1 template which is specified at the cross-connect point, the CEPT (2.048 MHz) template is specified at the transmit line output.
2. The template shown above is normalized. The actual pulse height is cable dependent and is specified in Table 3.
3. The corner points shown below are joined by straight lines to form the template.

MAXIMUM CURVE	MINIMUM CURVE
(0, 0.1)	(0, -0.1)
(109.5, 0.5)	(134.5, -0.2)
(109.5, 1.2)	(134.5, 0.5)
(244, 1.1)	(147, 0.8)
(378.5, 1.2)	(244, 0.9)
(378.5, 0.5)	(341, 0.8)
(488, 0.1)	(353.5, 0.5)
	(353.5, -0.2)
	(488, -0.1)

CHARACTERISTICS OF T1 AND CEPT INTERFACES Table 3

CHARACTERISTIC	T1	CEPT
LINE RATE	1.544 MHz	2.048 MHz
LINE CODE	AMI[1] or B8ZS	AMI or HDB3
TEST LOAD IMPEDANCE	100 Ohm Resistive	120 Ohm Resistive (wire pair) 75 Ohm Resistive (coax)
NOMINAL PEAK VOLTAGE	2.4 V to 3.6 V[2]	3.0 V (wire pair) 2.37 V (coax)
PULSE SHAPE	--Scaled to fit templates shown--	
NOMINAL PULSE WIDTH	324 ns.	244 ns.
PULSE IMBALANCE	< 0.5 dB difference between total power of positive and negative pulses.	1) Negative peak = positive peak peak +/- 5% 2) Positive width at nominal half amplitude = negative width at nominal half amplitude +/- 5%.

NOTES:
1. With a "ones" density of at least 12.5% and no more than 15 consecutive zeros.
2. Measured at the cross-connect (DSX-1) point; CSU applications may be 7.5 to 15 dB below these levels.

SUGGESTED TRANSFORMERS Table 4

MANUFACTURER	PART #	ISOLATION
AIE Magnetics - Nashville, TN	318-0720	1500V
Schott - Minneapolis, IN	10930	1500V
Pulse Engineering - San Diego, CA	FAL 33	1500V

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ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND   1.0V to +7V
OPERATING TEMPERATURE   0°C to 70°C
STORAGE TEMPERATURE   -55°C to +125°C
SOLDERING TEMPERATURE   260°C for 10°C.

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS   (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{DD}+.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
Supply	V_{DD}	4.75		5.25	V	

D.C. ELECTRICAL CHARACTERISTICS   (0°C to 70 C° V_{DD} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Supply current	I_{DD}		50		mA	2,3
Supply current	I_{DD}		35		mA	2,4
Supply current	I_{DD}		20		mA	2,5
Input Leakage	I_{IL}	-1.0		+1.0	uA	6
Output Current @ 0.4V	I_{OL}	+4.0			mA	7

NOTES:
1. All inputs except MTIP and MRING.
2. V_{DD} = 5.25v; TCLK = LCLK = 1.544 MHz; output line transformer and load as shown in Figure 2.
3. TAIS = 1
4. 50% "ones" density.
5. All "zeros" at data inputs.
6. 0.0V $<$ V_{IN} $<$ 5.0v
7. Output LF (open collector).

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CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL		MAX	UNITS
Input Capacitance	C_{IN}		5	pF
Output Capacitance	C_{OUT}		7	pF

A.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{DD} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
TCLK, LCLK Period	t_{CLK}		648		ns	1
TCLK, LCLK Period	t_{CLK}		488		ns	2
TCLK, LCLK Pulse Width	t_{RWH}, t_{RWL}		324		ns	1
TCLK, LCLK Pulse Width	t_{RWH}, t_{RWL}		244		ns	2
TCLK, LCLK Rise and Fall times	t_R, t_F			20	ns	
TPOS, TNEG Setup to TCLK falling	t_{STD}	50			ns	
LPOS, LNEG Setup to LCLK falling	t_{STD}	50			ns	
TPOS, TNEG Hold from TCLK falling	t_{HTD}	50			ns	
LPOS, LNEG Hold from LCLK falling	t_{HTD}	50			ns	

NOTES:
1. T1 applications
2. CEPT applications

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A.C. TIMING DIAGRAM Figure 5

Dallas Semiconductor
RECEIVE LINE INTERFACE
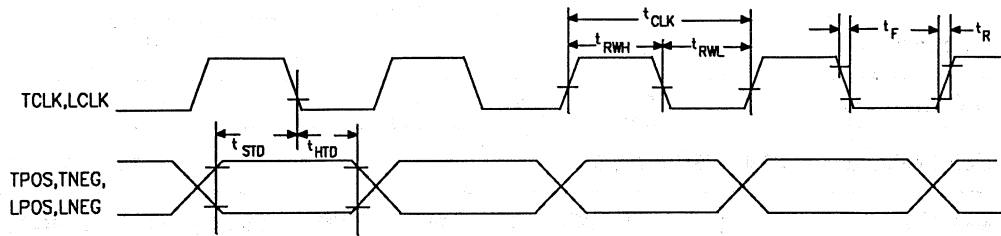
FEATURES

● Line interface for T1 (1.544 MHz) and CEPT (2.048 MHz) primary rate networks

● Extracts clock and data from twisted pair or coax

● Meets requirements of PUB 43801, PUB 62411 and applicable CCITT G.823

● Precision on-chip PLL eliminates external crystal or LC tank - no tuning required

● Decodes AMI, B8ZS and HDB3 coded signals

● Designed for short loop applications such as terminal equipment to DSX-1

● Reports alarm and error events

● Compatible with the DS2180A T1 and DS2181 CEPT Transceivers

● Companion to the DS2186 Transmit Line Interface

● Single 5V supply, low power CMOS technology

PIN CONNECTIONS

AVDD	1	18	DVDD
RAIS	2	17	RCL
ZCSEN	3	16	AIS
LCAP	4	15	BPV
RCLKSEL	5	14	NC
RTIP	6	13	RPOS
RRING	7	12	RNEG
LOCK	8	11	RCLK
AVSS	9	10	DVSS

6
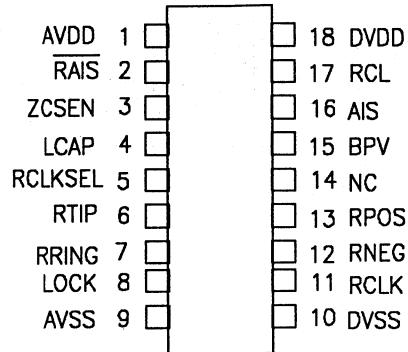
DESCRIPTION

The DS2187 interfaces user equipment to North American (T1 - 1.544 MHz) and European (CEPT 2.048 MHz) primary rate communication networks. The device extracts clock and data from twisted pair or coax transmission media and eliminates expensive discrete components and/or manual tuning

required in existing T1 and CEPT line termination electronics.

Application areas include DACS, CSU, CPE, channel banks and PABX to computer interfaces such as DMI and CPI.

DS2187 BLOCK DIAGRAM Figure 1
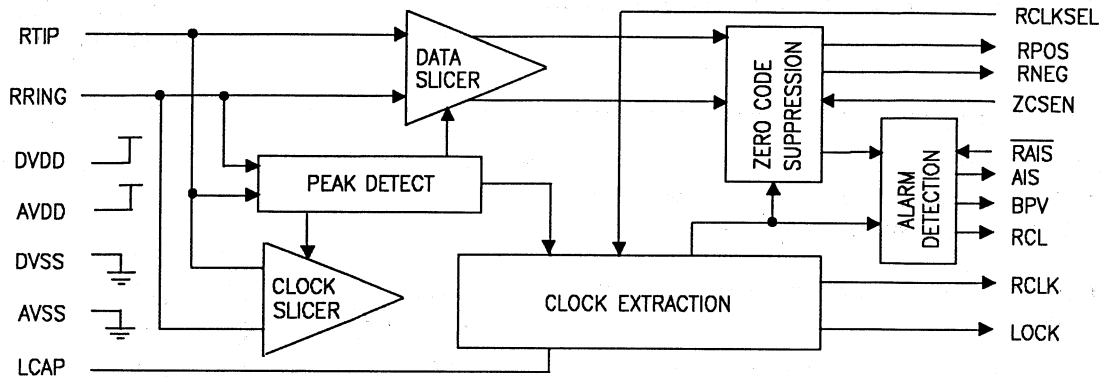
LINE INPUT
Input signals are coupled to the DS2187 via a 1:2 center-tapped transformer as shown in figure 2. For T1 applications, R1 and R2 must be 200 ohms in order to properly terminate the line at 100 ohms. R1 and R2 are set at 150 ohms for CEPT applications. Special internal circuitry of the RTIP and RRING inputs permit negative signal excursions below VSS, which will occur in the circuit in figure 2.

PEAK DETECTOR AND SLICERS
Signal pulses present at RTIP and RRING are sampled by an internal peak detect circuit. The data slicer threshold is set for 50% of the sampled peak voltage. The clock slicer threshold is set higher at 70% to prevent the negative undershoot of a worse case DSX-1 pulse from causing erroneous clocking.

Peak input levels at RRIP and RRING must exceed 0.6 volts to establish minimum slicer thresholds. Signals below this level will cause RCL to transition high after 192 bit times.

CLOCK EXTRACTION
The DS2187 utilizes both frequency locked

(FLL) and digital phase locked (DPLL) loops to recover data and clock from the incoming AMI signal. The DPLL characteristics differ for T1 and CEPT modes. T1 applications utilize a 18.528 MHz clock divided by either 11, 12, or 13 to match the phase of the incoming jittered line signal. This technique affords exceptional jitter tracking which enables the DS2187 to meet the latest AT&T PUB 62411 and ECSA jitter specifications. An 16.384 MHz clock divided by 7, 8, or 9 provides jitter tracking in the CEPT mode. The DPLL output is buffered and presented at RCLK. An on-chip laser trimmed voltage controlled oscillator (VCO) provides the precision 18.528 MHz and 16.384 MHz frequency sources utilized in the FLL. The FLL is a high-Q circuit which tracks the average frequency of the incoming signal, minimizing the effect of the DPLL on output jitter.

During the acquisition time or if RCL goes high, the LOCK pin will go low to indicate a loss of synchronization to the line signal. Once this pin goes high, the FLL has achieved frequency lock and valid data is present at the RPOS and RNEG outputs.

PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	AVDD	-	**Analog Positive Supply.** 5.0 Volts.
2	$\overline{\text{RAIS}}$	I	**Reset Alarm Indication Signal.** Every other falling edge at this input establishes the AIS alarm detection period.
3	ZCSEN	I	**Zero Code Supression Enable.** When high, incoming B8ZS (RCLKSEL = 0) or HDB3 (RCLKSEL =1) code words are replaced with all zeros at RPOS and RNEG; when low, no code replacement occurs.
4	LCAP	-	**Loop Cap.** Part of internal loop filter; attach a 10 microfarad capacitor from this pin to VSS.
5	RCLKSEL	I	**Receive Clock Select.** Tie to VSS for 1.544 MHz (T1) applications, to VDD for 2.048 MHz (CEPT) applications.
6 7	RTIP RRING	I	**Receive Tip and Ring.** Connect to line transformer as shown in figure 2.
8	LOCK	O	**Frequency Lock.** High state indicates that internal circuitry is phase and frequency is locked to the incoming signal at RRING and RTIP.
9	AVSS	-	**Analog Signal Ground.** 0.0 Volts.
10	DVSS	-	**Digital Signal Ground.** 0.0 Volts.
11	RCLK	-	**Receive Clock.** Extracted line rate clock.
12, 13	RNEG RPOS	O	**Receive Data.** Extracted receive data, updated on rising edge of RCLK.
14	NC	-	**No Connect.** Do not connect to this pin.
15	BPV	O	**Bipolar Violation.** Transitions high for the full bit period when a bit in violation appears at RPOS or RNEG; B8ZS or HDB3 code words are not accused when ZCSEN = 1.
16	AIS	O	**Alarm Indication Signal.** High when the received data stream has contained less than three zeros during the last two periods of the RAIS signal.
17	RCL	O	**Receive Carrier Loss.** High if 192 zeros appear at RPOS and RNEG, reset on next "one" occurrence.
18	DVDD	-	**Digital Positive Supply.** 5.0V.

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SYSTEM LEVEL INTERCONNECT Figure 2
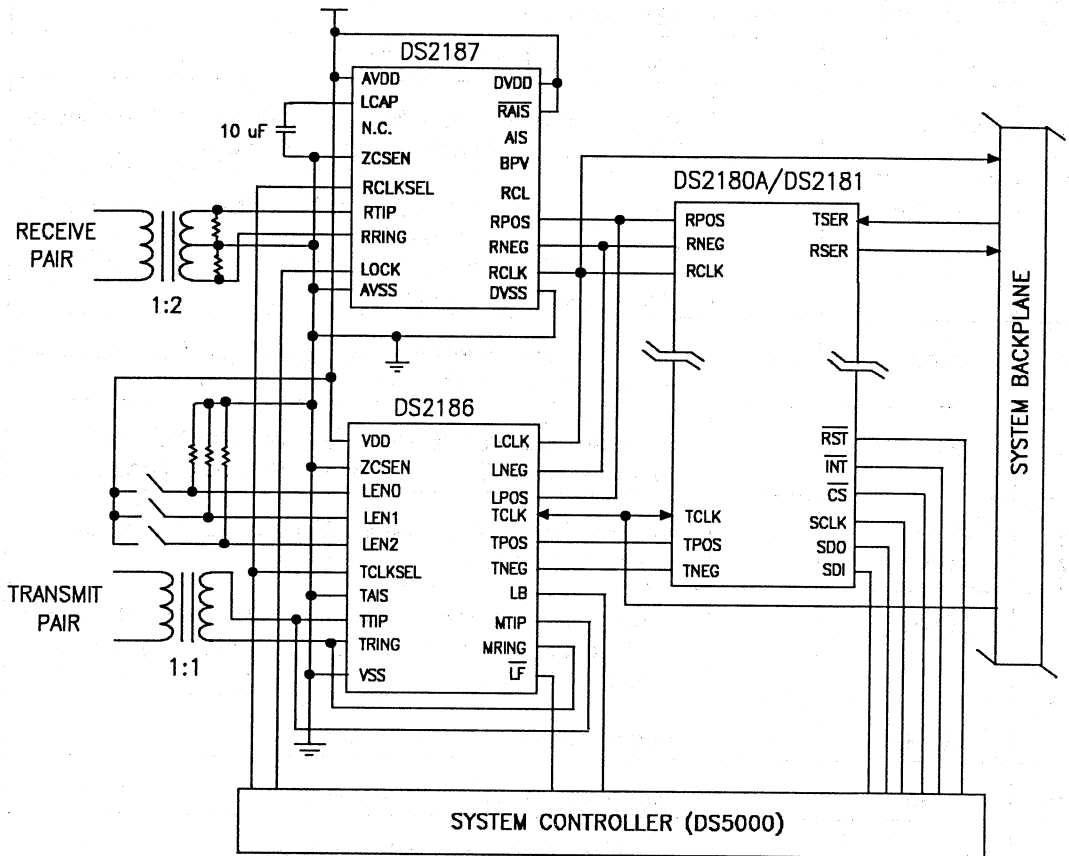
OUTPUT TIMING Figure 3
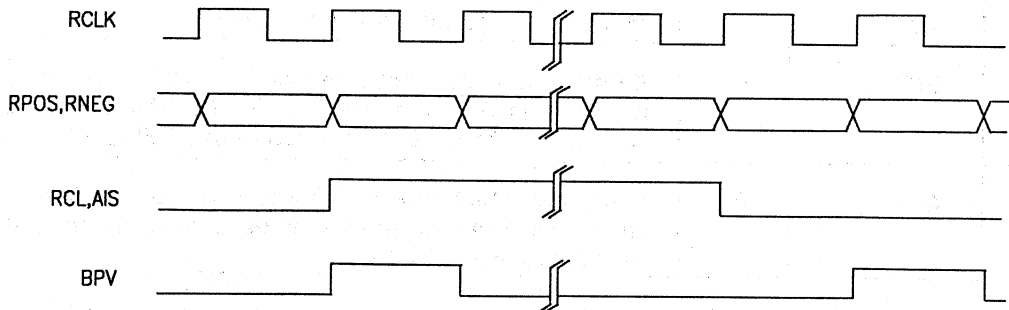
ZERO CODE SUPPRESSION

The device will decode incoming B8ZS (RCLKSEL = 0) or HDB3 (RCLKSEL = 1) code words and replace them with an all "0" code when ZCSEN = 1. When ZCSEN = 0, code words will pass thru the device without being altered. This feature can be disabled when the DS2187 is used with transceiver devices such as the DS2180A or DS2181.

ALARM DETECTION

The extracted data is monitored for network alarm and error conditions. RCL is set when 192 consecutive "zeros" occur; it is cleared on the next "1" occurrence. AIS is set when less than three "zeros" have appeared at RPOS and RNEG during the last two periods of the RAIS signal; once set, AIS will remain high for the next two periods of $\overline{RAIS}$. AIS will return low when greater than two "zeros" appear. BPV reports bipolar violations as they occur at RPOS and RNEG; B8ZS and HDB3 code words will not be flagged by BPV when ZCSEN = 1.

BYPASSING AND LAYOUT CONSIDERATIONS

The DS2187 contains both precision analog and high speed digital circuitry on the same chip. The power supplies of these circuits (AVDD, AVSS, DVDD and DVSS) should be connected to system analog and digital supplies. If separate system supplies do not exist, the appropriate supply pins may be tied together. The analog supply should be bypassed with 10 microfarad and 0.1 microfarad capacitors; if separate digital supply exists, bypass it with an additional 0.1 microfarad capacitor.

To assure optimum performance, the length of LCAP, RTIP and RRING printed circuit board traces should be minimized and isolated from neighboring interconnect.

6

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND**	-	-1.0V to +7V
OPERATING TEMPERATURE	-	0°C to 70°C
STORAGE TEMPERATURE	-	-55°C to 125°C
SOLDERING TEMPERATURE	-	260°C for 10 Sec.

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect reliability.
** Inputs other than RTIP and RRING.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX.	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{DD}+.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
Supply	V_{DD}	4.75		5.25	V	
RTIP, RRING Input Voltage Swing	V_{IN}	-7.0		12.0	V	

D.C. ELECTRICAL CHARACTERISTICS (0° C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Supply Current	I_{DD}		12		mA	2
Input Leakage	I_{IL}	-1.0		+1.0	uA	3
Output Current @ 2.4V	I_{OH}	-1.0			mA	4
Output Current @ 0.4V	I_{OL}	+4.0			mA	4

NOTES:
1. All inputs except RTIP and RRING.
2. Outputs open.
3. $0.0V < V_{IN} < V_{DD}$
4. All outputs.

ANALOG ELECTRICAL CHARACTERISTICS   (0° to 70°C, V_{DD} = 5V ±5%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Clock Acquisition	t_{LOCK}		20		ms	1
RTIP, RRING Minimum Sensitivity	V_{THRES}	.5	.6	.7	V_{pk}	2
FLL Loop Bandwidth	f_{BW}		50		Hz	3
Capture Range	f_{CAP}		± 6		%	4
Input Jitter Tolerance	J_{IN}	30			UI	5

NOTES:
1. Time from reappearance of a valid signal at RPOS and RNEG to a rising edge at LOCK.
2. Minimum peak voltage necessary for proper processing of signal.
3. Loop bandwidth when in lock (LOCK = 1).
4. When out-of-lock (LOCK = 0); measured as a percent of incoming clock frequency.
5. Maximum input jitter in unit-intervals at 10 Hz.

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CAPACITANCE   (t_A = 25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

A.C. ELECTRICAL CHARACTERISTICS (0° to 70°C, V_{DD} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
RCLK Period	t_{RCLK}	594	648	702	ns	1,3
RCLK Period	t_{RCLK}	427	488	549	ns	2,3
RCLK Pulse Width	t_{RWH}, t_{RWL}		324		ns	1
RCLK Pulse Width	t_{RWH}, t_{RWL}		244		ns	2
RCLK Rise and Fall Time	t_R, t_F			20	ns	
Propagation Delay RCLK to RPOS, RNEG	t_{PRD}			75	ns	
Propagation Delay RCLK or RRCLK to BPV, RCL, AIS	t_{PRA}			75	ns	
$\overline{RAIS}$ Pulse Width	t_{RAIS}	100			ns	

NOTES:
1. T1 applications (RCLKSEL = 0).
2. CEPT applications (RCLKSEL = 1).
3. Minimum and maximum limits shown reflect changes in DPLL divide ratio as required to track jitter.

A.C. TIMING DIAGRAM Figure 4
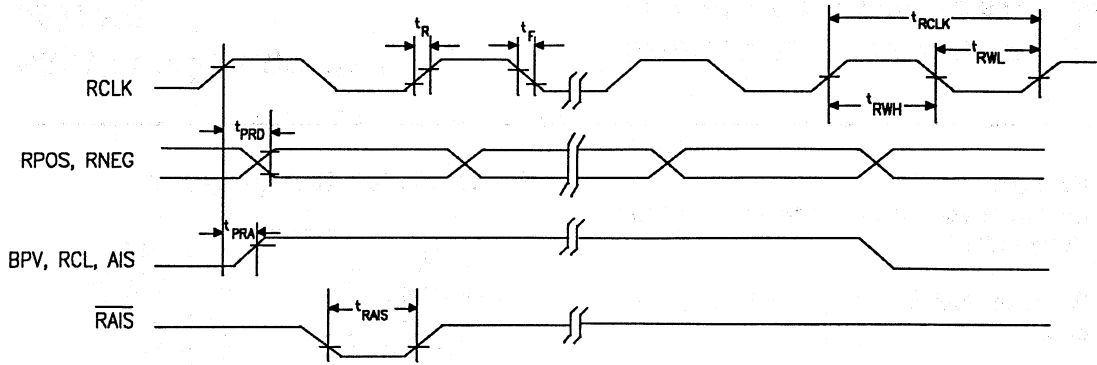
Dallas Semiconductor
Receive Line Interface
with Jitter Attenuation

FEATURES

- Line interface for T1 (1.544 MHz) and CEPT (2.048 MHz)

- Extracts clock and data from twisted pair of coax

- Meets requirements of PUB 62411, TR170, and CCITT recommendations

- Greater than 300UI of jitter tolerance at 10 Hz

- Jitter attenuation starting at 6 Hz

- Unique instantaneous jitter reporting through the serial port

- Decodes AMI, B8ZS, and HDB3 signals

- Designed for short loop applications such as terminal equipment to DSX-1

- Receiver sensitivity of 100 mv peak

- Simple serial interface port used for configuration and to report alarms and error events

- "Hardware" mode requires no host processor but still allows access to most features

- Compatible with the DS2180A T1 and DS2181 CEPT Transceivers

- Companion to the DS2186 Transmit Line Interface

- Single 5V supply, low power CMOS technology

- Available in 24-pin "skinny" DIP and 24-pin SOIC

PIN CONNECTIONS (tentative)
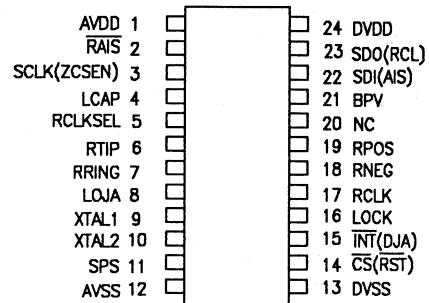
Pin	Signal		Pin	Signal
1	AVDD		24	DVDD
2	$\overline{RAIS}$		23	SDO(RCL)
3	SCLK(ZCSEN)		22	SDI(AIS)
4	LCAP		21	BPV
5	RCLKSEL		20	NC
6	RTIP		19	RPOS
7	RRING		18	RNEG
8	LOJA		17	RCLK
9	XTAL1		16	LOCK
10	XTAL2		15	$\overline{INT}$(DJA)
11	SPS		14	$\overline{CS}$($\overline{RST}$)
12	AVSS		13	DVSS

( ) = Hardware mode

FEATURES

- Modularized network interface for 1.544 Mbps T1 services

- "Network side" connects directly to T1 line

- Compatible with DS2180A transceiver

- Small size - approximately six square inches permits integration onto line cards

- Compatible with ATT publication 62411

- FCC Part 68 and Part 15 pre-registration

- Extracts clock and data with no external components or tuning

- Detects and generates in-band loopback codes

- Assures proper ones density to network

- Powered by a local +5 volt supply

PIN CONNECTIONS

TXTIP	○ 1	42 ○	RXTIP
TXRING	○ 2	41 ○	RXRING
NC	○ 3	40 ○	NC
NC	○ 4	39 ○	NC
LPWR+	○ 5	38 ○	NC
LPWR−	○ 6	37 ○	NC
NC	○ 7	36 ○	RSCOD
NC	○ 8	35 ○	RRCOD
RSTRLB	○ 9	34 ○	INHDEN
RCLK	○ 10	33 ○	REMLB
RPOS	○ 11	32 ○	TDENS
RNEG	○ 12	31 ○	TZERO
RZERO	○ 13	30 ○	TSCOD
CLKSEL	○ 14	29 ○	TRCOD
LB01	○ 15	28 ○	LOCLB
LB02	○ 16	27 ○	DELSEL
LB03	○ 17	26 ○	FRSYNC
LB04	○ 18	25 ○	TNEG
LB05	○ 19	24 ○	TPOS
LB06	○ 20	23 ○	TCLK
GND	○ 21	22 ○	VDD

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DESCRIPTION

The DS2190 is a small sealed module designed to meet the recommendations of ATT publication 62411 for interfacing to T1 1.544 Mpbs services (such as Accunet* T1.5, Skynet* T1.5 and High Capacity Digital Service). Because of the DS2190's FCC approval (Parts 68/15) and small footprint, T1 equipment makers can integrate an NIU into their products, reducing cost and increasing total system performance. Basic functions of the DS2190 are: clock and data recovery, isolation and surge protection, loopback detection and generation, and keep-alive signal generation. The DS2190 is compatible with D4 and ESF framing formats as well as B8ZS Clear Channel Coding. Also provided are alarm outputs for transmit and receive line status monitoring.

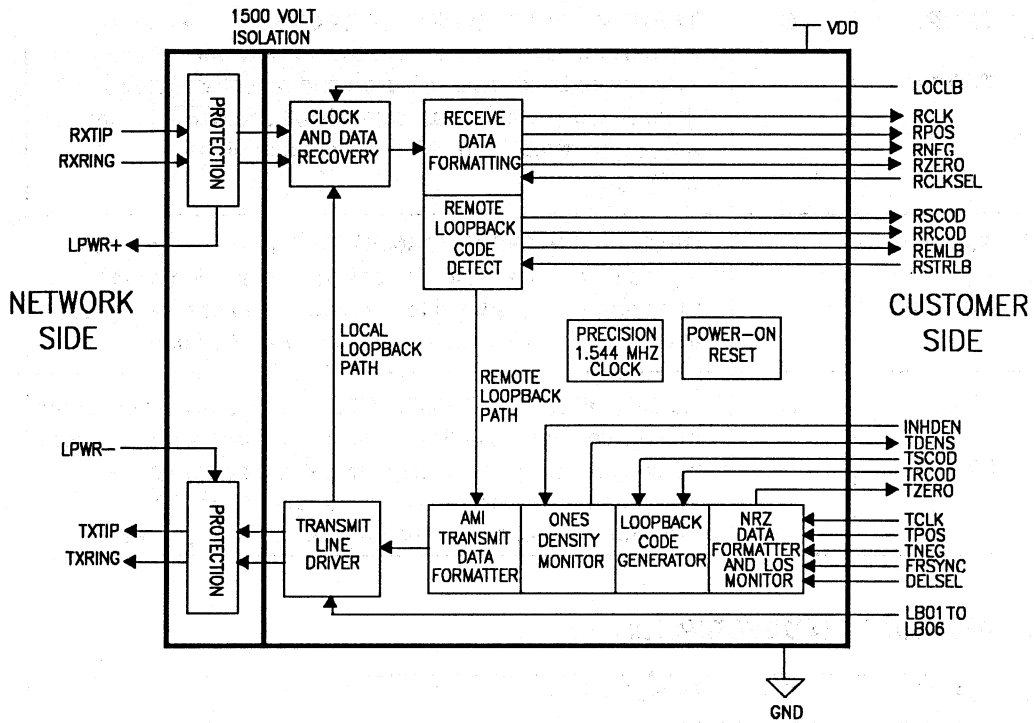*Service marks of AT&T Communications

The DS2190 Network Interface Unit (NIU) is a self-contained module which provides direct access to the T1 network. The *network* side of the module connects directly to the twisted pair. The *customer* side is a digital interface to the communication system. The module is functionally organized into a *receive* section and a *transmit* section. In addition, the module contains an on-board precision timing reference for keep-alive and monitoring functions, and an integral reset circuit to ensure proper operation at power-on. The module is powered from a single +5.0 volt source. If line-powering is provided by the carrier, this may be accessed at module pins. Figure 1 is a block diagram of the NIU module.

The AMI signal received from the network is passed through a Clock and Data Recovery circuit to extract the timing information. This circuit contains an integral automatic line-buildout (ALBO) circuit to compensate for cable loss. Alternately, the locally generated transmit signal may be looped back through this block to test the system equipment and the NIU module itself. The recovered clock and data are converted by the Receive Data Formatting circuit to a bipolar NRZ signal. This circuit also monitors the line for loss of signal. The formatted data is analyzed by the Remote Loopback Code Detect circuit for in-band maintenance loopback codes.

Data is fed to the transmit section as either a unipolar or a bipolar NRZ signal. The NRZ Data Formatter and LOS Monitor clocks in this data. It also generates a keep-alive signal in the event of an external clock failure. The Loopback Code Generator transmits in-band maintenance loopback codes to perform testing of the remote equipment and T1 span. The Ones Density Monitor ensures that the signal presented to the network meets the pulse density requirements. The AMI Transmit Data Formatter generates data pulses of the proper timing, which are transmitted onto the network by the Transmit Line Driver. Alternately, the received data will be transmitted back into the network if a remote loopback is enabled. The transmitted signal is also coupled back to the receive section for the local loopback.

DS2190 BLOCK DIAGRAM Figure 1

NETWORK-SIDE PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1 2	TXTIP TXRING	O	**TRANSMIT TIP AND RING OUTPUTS.** These are the transmit output connections to the T1 network. These outputs are transformer-coupled and reflect a source impedance of 100 ohms. Signal level and waveshaping are programmable through the strapping of the LBO inputs.
41 42	RXTIP RXRING	I	**RECEIVE TIP AND RING INPUTS.** These are the receive input connections to the T1 network. These inputs are transformer coupled and terminated at 100 ohms. Signals in the range of +0 to -30 dBSX can be applied here.
5 6	LPWR+ LPWR-	O	**LOOP POWER CONNECTIONS.** These pins connect to the internal center-taps of the transmit and receive transformers which provide access to the simplex d.c. power on the T1 line (if power is supplied by the carrier). These two pins should be tied together if the NIU is locally powered.

CUSTOMER-SIDE PIN DESCRIPTION Table 2

PIN	SYMBOL	TYPE	DESCRIPTION
9	RSTRLB	I	**RESET REMOTE LOOPBACK STATE.** The remote loopback state is reset when this pin is pulsed high. If this pin is strapped high, the DS2190 will never enter the remote loopback state.
10	RCLK	O	**RECEIVE CLOCK.** Recovered 1.544 MHz clock from the network.
11 12	RPOS RNEG	O	**RECEIVE BIPOLAR DATA OUTPUTS.** Recovered digital data. Updates occur on rising edges of RCLK and are latched for the full clock period. Bipolar violations from the network are preserved.
13	RZERO	O	**RECEIVE ZEROS.** This pin transitions high when there has been an absence of signal for 32 consecutive bit times. RZERO will return low when a valid signal pulse is detected at RXTIP and RXRING.

14	CLKSEL	I	**CLOCK SELECT.** If this pin is tied high, the RCLK output will switch to an internal 1.544 MHz clock when RZERO goes high (indicating a loss of signal). RCLK will revert to the normal recovered clock when RZERO goes low. If CLKSEL is tied low, RCLK will go to a low logic state when RZERO goes high.
15 - 20	LBO1 to LBO6	-	**LINE BUILD-OUT SELECT PINS.** Strapping these pins together determines the amount of attenuation for the transmit T1 signal. Refer to Table 3 later in this data sheet for proper settings.
21	GND	-	**SIGNAL GROUND.** 0.0 volts.
22	VDD	-	**POSITIVE SUPPLY.** 5.0 volts±5%. All module operations will cease if power is removed from this pin.
23	TCLK	I	**TRANSMIT CLOCK.** TPOS and TNEG inputs are sampled at the falling edge of this clock. TCLK also determines the TXTIP and TXRING pulse timings.
24 25	TPOS TNEG	I	**TRANSMIT BIPOLAR DATA INPUTS.** Data to be transmitted to the network.
26	FRSYNC	I	**FRAME SYNC INPUT.** 8 KHz clock which identifies F-bit positions in the TPOS and TNEG data stream. This clock is only used to preserve the F-bits when the transmit loopback code function is enabled.
27	DELSEL	I	**DELAY SELECT.** If this pin is strapped low, a rising edge on FRSYNC marks the beginning of the F-bit time on TPOS and TNEG. If this pin is strapped high, the rising edge of FRSYNC leads the F-bit by 10 bit times, which corresponds to the delay through a DS2180A.
28	LOCLB	I	**LOCAL LOOPBACK ENABLE.** The DS2190 enters the local loopback state when this pin is taken high, and the transmit signal is looped back to the receive clock and data recovery circuits. Meanwhile, TXTIP and TXRING will continue to operate normallly.

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29	TRCOD	I	**TRANSMIT RESET CODE.** When this pin is taken high, the in-band loopback reset code will be transmitted. This code consists of a repeating pattern of 001... that is overwritten by F-bit information.
30	TSCOD	I	**TRANSMIT SET CODE.** When this pin is taken high, the in-band loopback set code will be transmitted. This code consists of a repeating pattern of 00001... that is overwritten by F-bit information.
31	TZERO	O	**TRANSMIT ZEROS DETECT.** This pin will go high when the TCLK input has failed to transition for 150 ms. At this time, a keep-alive signal (AIS), consisting of a one in every bit position, will be transmitted to the network. The timing for this signal will come from an internal 1.544 MHz clock source.
32	TDENS	O	**TRANSMIT DENSITY VIOLATION.** A pulse will occur on this pin when a ones density violation has been detected in the transmit data.
33	REMLB	O	**REMOTE LOOPBACK DETECT.** This pin will transition high when the remote loopback state has been entered. It will return low when the DS2190 returns to normal operation. Remote loopback is entered by receipt of the in-band loopback set code for at least 4.75 seconds. It is terminated by either receipt of the in-band loopback reset code or the RSTRLB pin.
34	INHDEN	I	**INHIBIT DENSITY MONITOR.** If this pin is tied high, the DS2190 will not alter the transmit data to correct ones density violations. This pin should be strapped low to ensure that the ones density criteria is met unless the DS2190 is being used in a private network where this requirement does not apply.
35	RRCOD	O	**RECEIVE LOOPBACK RESET CODE.** This pin transitions high when the inband loopback reset code (a repeating "001" pattern) is being received, and will stay high as long as a valid reset code continues to be received.
36	RSCOD	O	**RECEIVE LOOPBACK SET CODE.** This pin transitions high when the inband loopback set code (a repeating "00001" pattern) is being received, and will stay high as long as a valid set code continues to be received.

NOTE: Do not connect to pins 3, 4, 7, 8, 37, 38, 39 and 40.

INTRODUCTION

In order to connect telecommunications equipment to a public T1 network, certain specifications must be met in the interface circuitry. The FCC has issued publication Part 68 for addressing concerns over network harm. That is, to make sure your equipment does not harm the network, whether it be the public switched telepone network or, in this case, the T1 network. Part 68 is also concerned about functionality of the interface circuit when exposed to a potential hazard such as lightning. The FCC has issued Part 15 in order to specify limits for EMI. However, for issues of performance, an accepted recommendation is AT&T Communications' Technical Reference 62411 (Oct 1985), hereafter noted as PUB 62411. This document addresses such issues as loopback, framing format, keep-alive signal, jitter and output pulse shaping. Compliance to these recommendations helps to ensure uniformity of performance when connecting to AT&T or any other T1 carrier. Also, a ANSI standard should soon emerge soon which will specify the required characteristics of a T1 network interface on a national level.

The DS2190 Network Interface Unit (NIU) is pre-registered with the FCC as an approved T1 network interface under Parts 68 and 15. What this means to a user is that with very little design effort an FCC-approved interface on a T1 line card can be implemented. The NIU is also functionally compatible with the relevant sections of PUB 62411. By adding a DS2180A T1 Transceiver and DS2176 Receive Buffer, a complete T1 line card can be designed, connecting an equipment backplane to a T1 carrier. An example of such an implementation is shown in Figure 3.

ISOLATION

One of the primary functions of the DS2190 is to provide galvanic isolation between the network and the customer premise equipment (CPE).

The network-side pins (1,2,5,6,41, and 42) have at least 1500 volts D.C. isolation from all customer-side pins. In order to maintain this isolation, all PCB traces to the network-side pins should be at least 200 mils away from any normal board trace (i.e. logic or system traces). The network-side traces should be at least 20 mils wide and should be as short as possible. Typically, for a T1 line card application, the DS2190 should be very close to the physical T1 connector (RJ48C or similar connector). If the T1 connector is not on the same PCB as the DS2190 then locate the DS2190 near the network connection leads at the backplane inputs.

POWERING

The functions performed by the DS2190 network interface unit (NIU) are critical to the operation of the T1 network. If power is removed from the NIU, it will cease to produce a T1 signal and oscillation in the line repeaters could occur. For this reason, the NIU's VDD pin should be connected to a non-interruptable power source. There are two methods for providing this non-interruptable power source: line powering and local powering.

In many cases the T1 carrier provides a simplex D.C. current for line powering. Access to this power source is available at the NIU's LPWR+ and LPWR- pins. Because the D.C. power source on a typical T1 line is current-limited to 60 mA, a switching D.C.-D.C. converter will be necessary to be able to power the DS2190. For FCC approval, this converter must meet all provisions of Part 68 for isolation and Part 15 for EMI. Contact the Telecom marketing group for assistance in such an application.

In new applications, the FCC permits local powering of the NIU. This local power should be battery-backed in the event of a CPE power failure so that the DS2190 can still function. When local powering is used, the LPWR+ and LPWR- leads should be tied together to permit

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pass-through of the D.C. power loop.

Exercise extreme caution with these pins since voltages in the range of +130 to -130 volts could exist here.

RECEIVE DATA PROCESSING

Receive signals from the T1 network are coupled to the DS2190 by connecting RXTIP and RXRING to the T1 receive pair. Signals in the range of +0 dBSX to -30 dBSX can be applied here (typically, a carrier will limit signals to a range much less than this). The receive interface includes clock and data extraction with an integral ALBO (automatic line-build out) circuit which adjusts for loop length of up to 6000 feet of 22-gauge ABAM cable. The extracted clock and data are formatted and presented at the RCLK, RPOS, and RNEG pins. The RCLK will be nominally 1.544 MHz at a 50% duty cycle. RPOS and RNEG are the recovered bipolar data in a non-return format (i.e. valid for an entire RCLK cycle), and may be sampled on the falling edge of RCLK.

The network timing is conveyed in the received data pulses, and long strings of zeros will cause timing synchronization to be lost. When the DS2190 detects 32 consecutive zeros at RXTIP and RXRING, it brings the RZERO pin high. If the CLKSEL pin is strapped low, the RCLK output will go low at this time. If the CLKSEL pin is strapped high, RCLK will be switched to an onboard 1.544 MHz timing reference. As soon as a data pulse is detected at either the RXTIP or RXRING input, the RZERO pin will return low and RCLK will return to the extracted clock signal.

REMOTE LOOPBACK CODE PROCESSING

The DS2190 recognizes the in-band codes which control remote loopbacks at the DS-1 level. The code to enter (set) the remote loopback state is a repeating "00001" pattern. The code to leave (reset) the remote loopback state is a repeating "001" pattern. These codes may be either framed or unframed. After receipt of a valid set code for approximately 4.75 seconds, the DS2190 enters a loopback condition. The REMLB output will transition high, and the received data will be transmitted as-is through TXTIP and TXRING. The received data will continue to appear at RPOS and RNEG as normal. While in loopback, the data at TPOS and TNEG will be ignored. Once in the remote loopback state, the set code from the network need not be sustained.

After receipt of a valid reset code for approximately 4.75 seconds, the DS2190 will return to normal operation. The REMLB output will return low and the information at TPOS and TNEG will be processed as normal.

The remote loopback sequence may be monitored at the RSCOD and RRCOD pins. They indicate reception of a valid set and reset code, respectively. These pins transition high when a valid code has been received for approximately 680 ms and remain high as long as a valid code is detected. This is illustrated in figure 2A.

The RSTRLB pin resets the remote loopback state. If this pin is strapped high, the DS2190 will never enter the remote loopback state. If this pin is pulsed high while the DS2190 is in the remote loopback state, it will return to normal operation. If RSTRLB is activated while the DS2190 is in a remote loopback state and a valid set code is still being received, the current set code sequence will not trigger the remote loopback state again. The RSCOD and RRCOD pins are not effected by the RSTRLB pin. This is illustrated in figure 2B.

Loopbacks are used to isolate network problems. To aid in this diagnosis, the DS2190's loopback code detectors are tolerant to abnormally high error rates, even up to a 10^{-2} bit error rate.

REMOTE LOOPBACK PROCESSING Figure 2
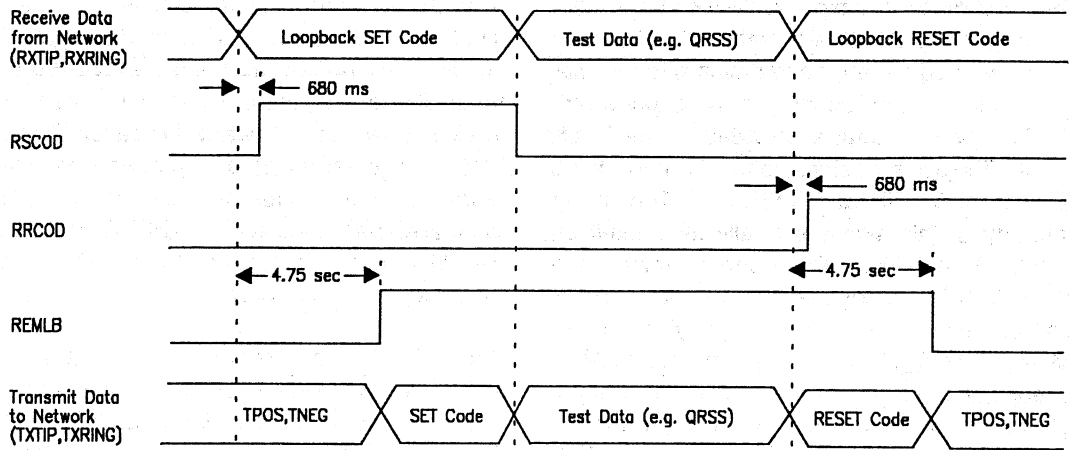
(A) Remote Loopback Code Handling
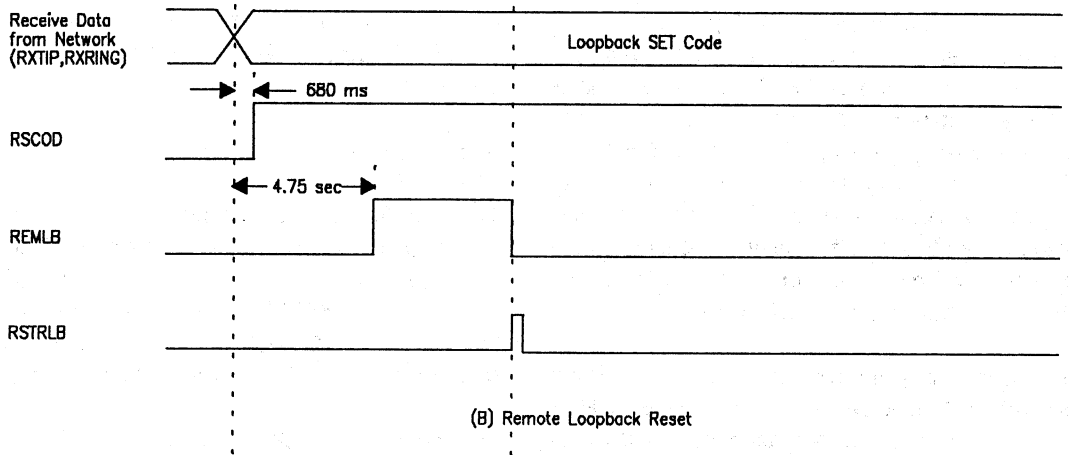
(B) Remote Loopback Reset

TRANSMIT TIMING REQUIREMENTS

Data to be transmitted into the network is presented at the TPOS and TNEG inputs. Normally this input data is in a bipolar, NRZ-coded format. Although the DS2190 allows these two inputs to be connected together and driven with unipolar data, the bipolar configuration is preferred. Timing for this data is provided at the TCLK input. The transmit signal to the T1 network will appear at TXTIP and TXRING. The timing integrity of this signal is totally dependant on TCLK. To meet FCC Part 68 requirements and PUB 62411 recommendations, the TCLK source must have a frequency of 1.544 MHz±64Hz (±48ppm). The emerging ANSI specification will probably require an accuracy of ±50Hz (about ±32ppm) for new equipment. Therefore, it is recommended that the TCLK clock source be accurate to at least ±50Hz to meet all existing and proposed standards.

The duty-cycle of the TCLK input is also very important since a T1 pulse is nominally 324 nsec in width (half the 1.544 MHz). A duty cycle of 50% ±1% is required to meet the network pulse template requirements. The DS2190 will perform all necessary wave-shaping to conform to these specications given that the duty-cycle requirements are met. The output pulse characteristics will meet the specifications in section 5.4.4 and figure 2.4 of PUB 62411.

Another important requirement of the TCLK source is that it be relatively jitter-free. PUB 62411 recommends a maximum of 0.05 unit-intervals peak-to-peak (Ulpp) measured without bandlimiting. This document describes other jitter limits measured in specific frequency bands. For full complaince to AT&T recommentations on output jitter, please see this publication. Jitter specifications are undergoing study by several organizations and these requirements may change in the future. However, a TCLK input with less than 0.05 Ulpp of total jitter should meet existing and proposed recommendations from a T1 network interface.

TRANSMIT LOSS OF SIGNAL

If the DS2190 detects no transitions at the TCLK input for 150 msec, a loss of signal (LOS) condition will be declared and the DS2190 will transmit a blue alarm to the network. This alarm is also known as an "Alarm Indication Signal" (AIS) and consists of an unframed all ones pattern. The timing for the AIS is based on the internal reference clock. The TZERO output will transition high to indicate that the DS2190 has declared a LOS condition.

The DS2190 recognizes the loss of TCLK signal within approximately 5 µsec (8 clock intervals), and switches transmit timing control from the TCLK input to the internal reference. This guarantees that between this time and the declaration of a LOS condition, the DS2190 will still generate a signal which meets the network ones density requirements. As soon as a pulse is detected at TCLK, the DS2190 returns to normal operation.

REMOTE LOOPBACK CODE TRANSMISSION

The DS2190 may transmit the codes to place the remote digital terminating equipment (DTE) into a loopback state. This feature is controlled with the TRCOD and TSCOD pins. Please refer to the "REMOTE LOOPBACK CODE PROCESSING" section for information on these codes.

The remote loopback codes are framed, in-band patterns. The FRSYNC input indicates the position of the framing bit at the TPOS and TNEG inputs. This bit overwrites the loopback code in the transmitted data. When the DELSEL pin is strapped low, the frame bit occurs at the bit position of the FRSYNC pulse. When DELSEL is strapped high, the frame bit occurs 10 bit positions later than the FRSYNC pulse, which corresponds to the delay through a DS2180A. If FRSYNC is strapped high or low, an unframed

pattern will be produced, irregardless of the DELSEL strapping.

The DS2190 is fully transparent to B8ZS encoding; all data (including bipolar violations) are passed to the network as presented at TPOS and TNEG. When the DS2190 is transmitting a remote loopback code, a frame bit which has been altered from a zero to a one by an external B8ZS encoder will be received as a one by the remote equipment. This is because the remainder of the B8ZS code word is overwritten by the loopback code. To maintain framing at the remote equipment, B8ZS encoding should be inhibited while TRCOD or TSCOD are active. Note, however, that the DS2190 is able to recognize loopback codes even in the presence of framing errors.

TRANSMIT PULSE DENSITY

The term "pulse density" (also called "ones density") refers to the number of ones present in the T1 signal. With bipolar signals, a pulse is only present when a one is to be transmitted; a zero is represented by the absence of a pulse. Therefore, when a long string of zeros is to be transmitted in a bipolar fashion, there is no signal present on the line during this time. This can lead to excessive jitter or even failure in the repeater clock recovery circuits if these strings of zeros are not controlled in length and in density. The DS2190 ensures that its outgoing transmit signal (present at TXTIP and TXRING) meets the pulse density recommendations in PUB 62411, which are as follows:

1) no more than 15 zeros in a row, and
2) at least N ones in every time window of $8(N+1)$, where $1 \leq N \leq 23$.

The DS2190 will monitor the data at TPOS and TNEG to ensure that these requirements are met. If the DS2190 detects a pulse density violation, it will signal this condition by a one-bit period pulse on the TDENS˙ output. If the

INHDEN pin is strapped low, a one will be inserted into the transmitted data to ensure the pulse density conditions are met. If the INHDEN pin is strapped high, the data will not be altered.

Note that a signal with B7 zero-supression or B8ZS coding will always meet these requirements, and therefore will not be altered by the DS2190. However, in the event of TCLK loss, INHDEN must be low to guarantee that the ones density criteria is met during the interval from TCLK loss to the declaration of a transmit LOS condition.

TRANSMIT LBO SELECTION

Line build-out (LBO) is the process of inserting into the transmit path a circuit which simulates the characteristics of a certain length of wire. The DS2190 contains three LBO circuits which provide 0dB, 7.5dB, or 15dB of attenuation at 772 KHz (the center of the signal spectrum), which cover cable lengths from 0 to 6000 feet. The characteristics of these circuits conform to FCC Part 68 recommendations. In most applications, LBO selection is determined at the time of installation of the CPE by a telephone craftsman. It is recommended that a mechanical switch be installed on the board that is easily accessible and clearly marked to indicate the proper settings. The switch should strap the appropriate LBO pins together for the corresponding cable loss as shown in Table 3.

LBO Strapping Chart Table 3

For equivalent loss at 772 KHz,	strap these inputs together.
0.0dB	LB01 to LB06
7.5dB	LB01 to LB02
	LB05 to LB06
15.0dB	LB01 to LB02
	LB03 to LB05
	LB04 to LB06

TYPICAL T1 LINE CARD APPLICATION Figure 3
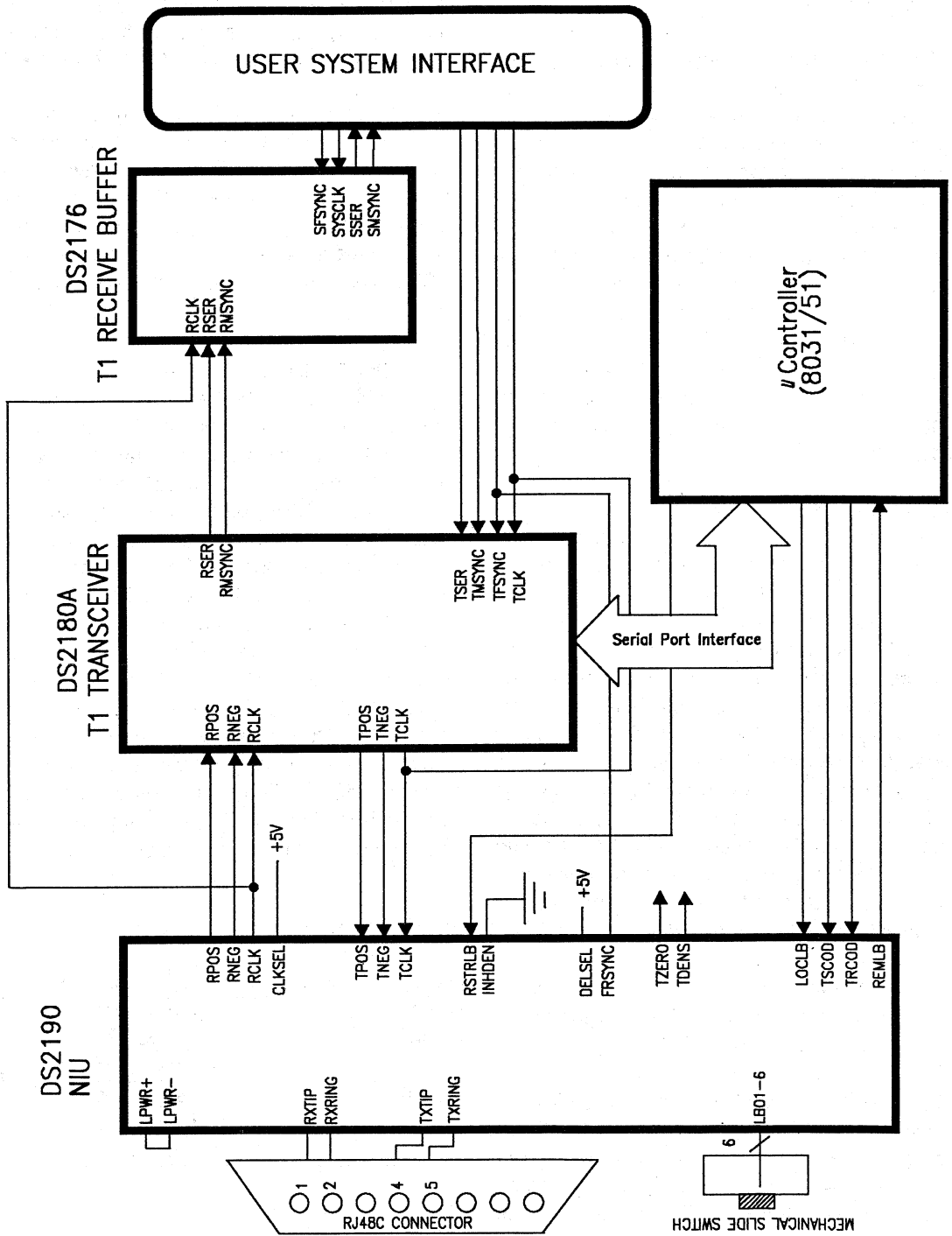
FAULT ISOLATION WITH LOOPBACKS

At some time a communications link will fail. Any number of events can cause a failure: a connector may fall out of place, construction work might sever a cable, etc. One of the most important features communications equipment can offer is the ability to locate and isolate problems quickly.

Fault isolation is commonly done by employing loopbacks. When a piece of equipment is placed into a loopback mode, it will echo the received data back to the sender. The sender may compare this data with the original transmitted data. If they compare, then the span is probably functional at least this far. If the data streams differ, then a failure has been localized in the equipment or lines in the loopback path. Figure 4 illustrates this methodology.

The DS2190 Network Interface Unit (NIU) can play an important part in fault isolation. It provides several loopback testing features. Equipment which incorporates the DS2190 as its interface to the T1 network may easily avail itself of these features.

The NIU offers two types of loopbacks. The first kind is called a "local loopback." A local loopback is used to test the local data terminating equipment (DTE) nearly up to the network interface. This includes testing of the digital and analog functions of the NIU. The second kind of loopback is called a "remote loopback". This loopback tests the connection across the network span and into the remote DTE. AT&T technical reference 62411 (ACCUNET* T1.5 Service Description and Interface Specifications, Oct 85) describes this type of loopback in section 5.2.1. Additional details are given in section 2.1.2 of AT&T technical reference 54016 (Requirements for Interfacing Digital Terminal Equipment to Services Employing the Extended Superframe Format, Mar 86). This latter document calls this sort of loopback a "line loopback" (LLB). The NIU conforms to the requirements in both of these documents.

A major drawback to testing via loopbacks is that the communications link must be taken out of service to perform this testing. In the case of a local loopback, the local DTE is occupied with the test data and is unable to process the data from the network. In the case of a remote loopback, the DTE on both sides of the T1 span and the span itself are occupied with the test data.

Figure 1 shows a block diagram of the NIU. The "customer-side" of the NIU is the digital interface to the equipment. The "network-side" of the NIU connects to the T1 line. Note that the block diagram indicates the data paths for both types of loopbacks. The reader should be familiar with the basic operation of the NIU and the function of the pins shown in this figure.

LOCAL LOOPBACK TESTING

The NIU is placed into a local loopback state by bringing the LOCLB pin to a high level. In this state, the signal from the transmit drivers is fed back into the receive clock and data extraction circuitry. The loopback path travels through the entire digital and analog circuitry of the NIU. Therefore, local loopbacks may be employed to perform a very thorough test of the local equipment including the NIU itself.

REMOTE LOOPBACK PROCESSING

In order to perform remote loopback testing, the equipment on both sides of the T1 line must cooperate. One piece must generate the loopback control commands, generate the test data, and monitor the results. The other piece must recognize and respond to the loopback control commands. In our discussion, we will call these two pieces of equipment the "originating equipment" and the "responding equipment," respectively.

There are two code signals used to control the loopback state of the responding equipment: an

"activate code" and a "deactivate code". These codes are sometimes called the "set code" and the "reset code". To enable a loopback at the responding equipment, the originating equipment must transmit the set code for at least five seconds. Once the responding equipment has enabled the loopback, the set code need not be sustained, and network testing may commence. Once testing is completed, the originating equipment will transmit the reset code for at least five seconds, which should cause the responding equipment to disable the loopback and return to normal operating conditions.

Both loopback codes are a framed, in-band pattern. This means that the codes replace the data carried in the T1 packet, but every 193rd bit may be overwritten by the T1 F-bit. (We use the term "F-bit" to include both the 12 framing bits in the D4 standard and 24 S-bits in the ESF standard.) The responding equipment must recognize these codes whether or not the 193rd bit in the pattern has been altered with F-bit data. The "set code" is a repeating "00001" pattern, and the "reset code" is a repeating "001" pattern.

The NIU supports remote loopbacks at either side of the network. When it is in the originating equipment, it may generate the loopback code. When it is in the responding equipment, it will recognize and respond to the loopback codes.

THE NIU AS ORIGINATOR

When the NIU is in the originating equipment, it is used to transmit the loopback codes. This function is controlled with the TSCOD (transmit remote loopback set code) and TRCOD (transmit remote loopback reset code) pins. When both of these pins are low, the NIU takes the system data from pins TPOS and TNEG, and transmits this data into the network through pins TXTIP and TXRING. When one of these pins is brought high, the NIU stops transmitting system data and begins to transmit the appropriate remote loo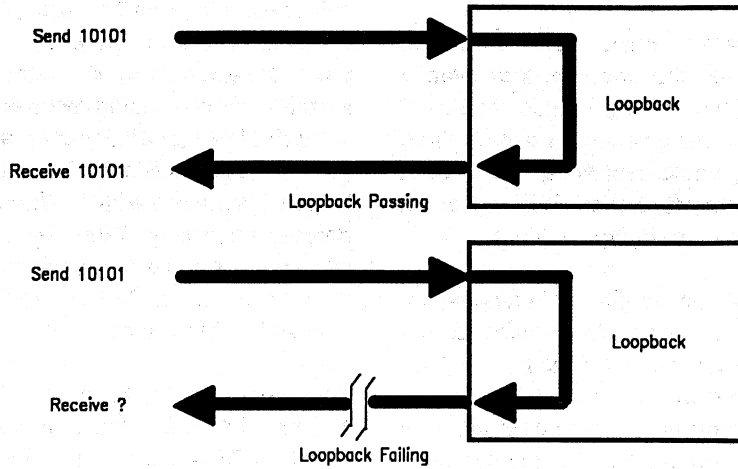pback code. The TCLK pin is the timing source for the transmitted data even when a loopback code is being transmitted. Avoid the condition where both TSCOD and TRCOD are high simultaneously.

The F-bit data which overwrites the loopback code is taken from the NIU's TPOS and TNEG inputs. A rising edge on the FRSYNC input locates the position of the F-bit. When the DELSEL input is strapped low, the NIU will sample TPOS and TNEG for the F-bit data at the next TCLK falling edge following the FRSYNC rising edge. When the DELSEL input is strapped high, the NIU will sample TPOS and TNEG for the F-bit data at the eleventh TCLK falling edge following the FRSYNC rising edge. This latter case introduces a 10-bit delay, which accounts for the delay through a DS2180A. Figure 5 illustrates why this delay is required when a DS2180A is connected to the NIU.

The B8ZS coding technique is commonly used in T1 communications to guarantee that the network restrictions on long intervals of zeros are not violated. The advantage to B8ZS encoding is that it does so without corrupting data bits. Instead, it replaces a string of eight consecutive zeros with a special 8-bit code word. This code word contains bipolar violations which do not occur in normal communications data. The equipment which receives the B8ZS code word will restore it back to eight zeros. The NIU always passes bipolar violations through unchanged, so B8ZS encoding may be used.

When either TSCOD or TRCOD is enabled, the TPOS and TNEG inputs are ignored except for the F-bit. If the F-bit is a zero within a string of eight or more zeros, then it may have been altered by an external B8ZS encoder. The NIU will pick up this altered F-bit, and place it in the transmitted data. However, the F-bit will now be surrounded with the loopback code and not the B8ZS code word, and therefore the responding equipment will not know that this bit should be

USING LOOPBACKS FOR NETWORK DIAGNOSIS Figure 4

Send 10101

Loopback

Receive 10101

Loopback Passing

Send 10101

Loopback

Receive ?

Loopback Failing

TRANSMIT USING DS2180A Figure 5

VDD

DS2190 NIU

TPOS
TNEG
TCLK
FRSYNC
DELSEL

TXTIP
TXRING

DS2180A TRANSCEIVER

TPOS   10-CLOCK
TPOS   DATA DELAY

FROM
SYSTEM
BACKPLANE

TSER
TCLK
TFSYNC
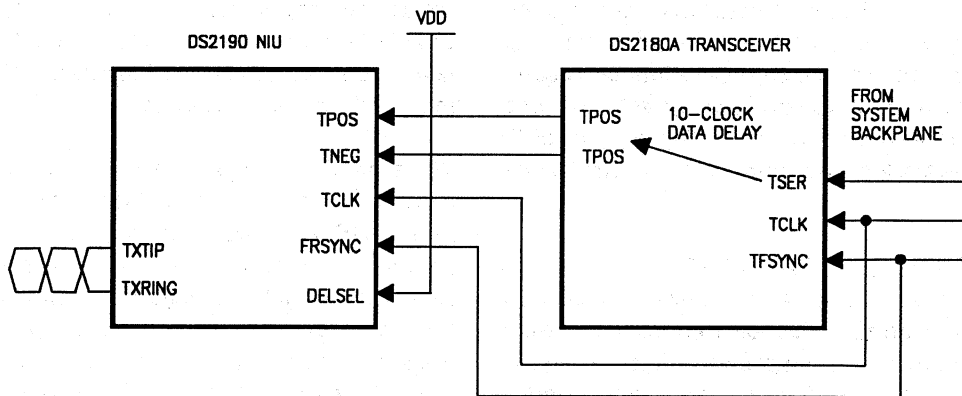
restored to a zero. Instead, it will see an errant bipolar violation and possible framing error.

None the less, the responding equipment should be able to recognize the loopback code even in the absence of valid framing, so this should not be a problem. If framing needs to be maintained at the responding equipment while the loopback code is being transmitted, then B8ZS encoding should be suppressed during this time.

From the point of view at the originating equipment, network testing should proceed as follows. First, the NIU TSCOD pin is held high for at least five seconds. This will place the responding equipment into a loopback state. Now TSCOD may be returned to its inactive (low) state. A test pattern may now be applied to the TPOS and TNEG pins. The NIU will transmit this data onto the network. The responding system should receive this test pattern and transmit it back to the originating system. Therefore, the RPOS and RNEG output pins may be monitored for this test data, time displaced by the round-trip network delays. Once testing has been completed, the TRCOD pin should be activated long enough to allow the responding equipment to disable the loopback and return to normal service.

THE NIU AS RESPONDER

When the NIU is in the responding equipment, it must recognize the loopback codes and loop the data back to the originator. This function is performed automatically. The data received at the RXTIP and RXRING inputs is analyzed for the loopback codes. These codes will be recognized whether or not the pattern has been overwritten with F-bit data. In addition, the code monitor is extremely tolerant to line noise. The NIU will recognize the loopback codes even if the bit errors due to line noise is at a 10^{-2} bit error rate.

There are three outputs from the code recognizer circuitry: RSCOD, RRCOD, and REMLB. All of the pins are normally low. The RSCOD output will go high when the loopback set code is detected on the incoming data stream for approximately 680msec. It will stay high as long as a valid set code is being received. The RRCOD output is similar, but it detects the loopback reset code. The REMLB output indicates the remote loopback state of the NIU. When low, the NIU is operating normally. When REMLB is high, the NIU is in a remote loopback state, and all the data it receives at RXTIP and RXRING will be echoed back to the network.

The remote loopback state is entered when the NIU has detected a valid set code for approximately 4.75 seconds, or approximately 4.07 seconds after RSCOD transitions high. Once the NIU is in a loopback state the set code need not be sustained, the NIU will stay in the loopback condition until the originator sends the loopback reset code. If the NIU detects a valid reset code for approximately 4.75 seconds, it will disable the loopback and return to normal operation. If the NIU is not in a loopback state, the reset code will have no effect.

While the NIU is in a remote loopback state, the data at inputs TPOS and TNEG are ignored. The RPOS and RNEG outputs will continue to produce the data received from the network. Note that the NIU block diagram shows that the remote loopback data path bypasses all of the transmit data monitoring functions. For example, ones density violations present in the received data will not be detected or corrected; they will be transmitted back to the originator. While the NIU is in loopback, it simply regenerates the received data and echoes it back to the network as it. Even bipolar violations in the received data will be preserved.

The RSTRLB input may be used to force the NIU out of a loopback condition or inhibit it from going into a loopback condition. If this pin is strapped

low, the NIU will respond to all set and reset codes as described above. If this pin is strapped high, the NIU will never go into a loopback state. In this mode, the NIU will continue to detect the loopback codes and indicate such detection at the RRCOD and RSCOD outputs, but the REMLB pin will never go high and the NIU will always stay in normal operating mode. If the NIU is in a loopback condition, a high level at the RSTRLB input will bring the REMLB output low and return the NIU to normal operation. If the NIU is not in a loopback condition, RSTRLB will have no effect. Figure 6 details how the remote loopback detection circuitry works.

A SYSTEM EXAMPLE

We shall now consider an example where a remote loopback is used to test a T1 network connection. The system we shall examine is shown in Figure 7. The NIU will be used as the interface to the network in both the originating equipment and the responding equipment. This will allow us to see how it functions in both roles. A QRSS tester will be connected to the originating equipment. This tester will be used once a loopback has been established to perform bit error-rate (BER) testing. The tester will generate a quasi-random data stream which will be transmitted to the network. The returned data will be analyzed by the tester to ensure that the data hasn't been changed, only displaced in time.

The scheme for our test will be as follows:

(1) Transmit the loopback set code from the originating equipment.
(2) Wait for the responding equipment to go into the loopback condition.
(3) Perform the line testing.
(4) Transmit the loopback reset code from the originating equipment.
(5) Wait for the responding equipment to return to normal operation.
(6) Terminate the test procedure.

The results of this test scheme are show in figure 8. We shall go through the illustrated waveforms step by step to see how the testing was performed.

The first step is to transmit the loopback set code. At time "A" the TSCOD pin of the originating NIU was brought high. Almost immediately the transmitted data stream switched from the normal data to this loopback code. Hopefully the receiving NIU is now receiving the loopback set code and has begun its 4.75 second countdown.

Shortly after time "A" (680msec later), the RSCOD pin of the responding NIU transitions high. This is our first indication that a remote loopback is about to be enabled.

At time "B", which is approximately 4.75 seconds after time "A", the responding NIU goes into a loopback state. The REMLB output transitions high and the transmitted data at TXTIP and TXRING is now the received data echoed back to the network.

At time "C", the TSCOD pin of the originating NIU returns to its inactive state, and line testing begins. We won't be changing any of the NIU control inputs during the test interval. Note that once the originating NIU started sending the test data instead of the loopback set code, the responding NIU detected the end of the loopback code sequence and RSCOD returned low.

There is a very curious occurrence between times "B" and "C." Notice that the RSCOD output of the originating NIU transitions high. This happens because the responding NIU is echoing the loopback set code back to the originating NIU, and the detection circuitry in the originating NIU has started its own 4.75 second countdown. It is very important that the set code sequence is interrupted before the countdown is finished, otherwise the originating NIU will go

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REMOTE LOOPBACK DETECTION LOGIC Figure 6
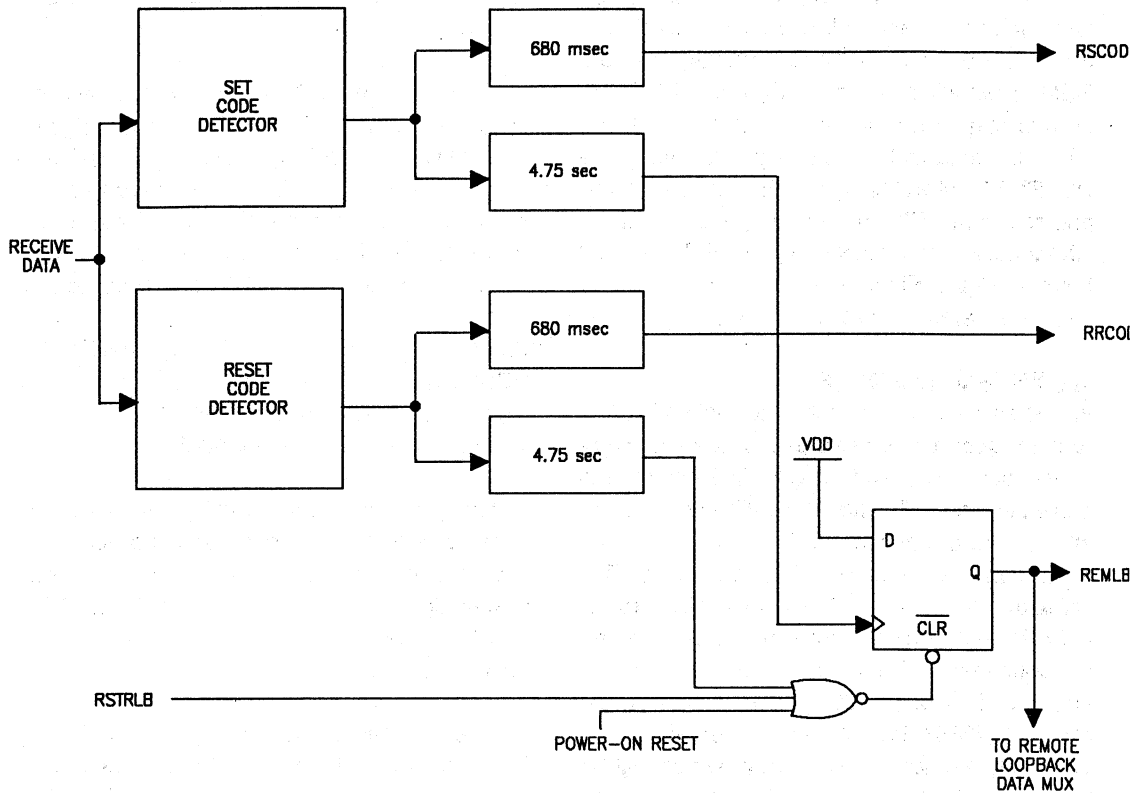
SYSTEM EXAMPLE BLOCK DIAGRAM Figure 7
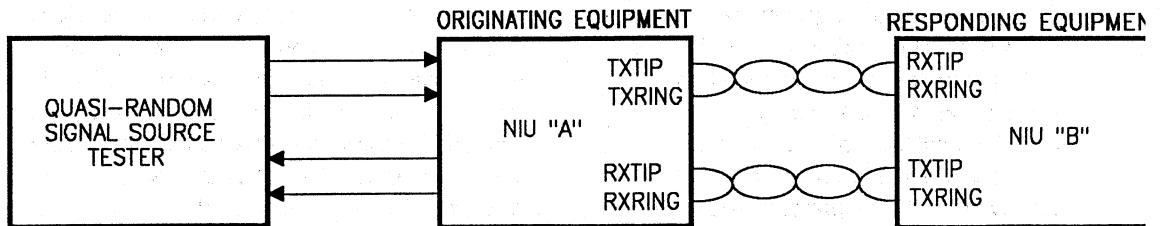
into loopback itself. Once this happens, a closed data loop will be formed, and the only to break the loop is by activating the RSTRLB pin on either NIU.

This circumstance suggests that the set code should be transmitted by the originating NIU for at least 4.75 seconds (to ensure that the responding NIU enables loopback), but it shouldn't be transmitted more than 9.50 seconds (to ensure that the originating NIU doesn't go into loopback itself.

An alternative is to take advantage of the loopback code recognition in the originating NIU. In this case we will use the RSCOD output of the originating NIU to tell us when the responding equipment has enabled the loopback. Figure 9 shows a circuit which will do this. A rising edge on the ENTSCOD input begins transmission of the remote loopback set code. When the responding equipment goes into a loopback state, RSCOD will latch the RREMLB output high and return TSCOD low. Therefore, the originating equipment need only pulse ENTSCOD high and wait for RREMLB to go high.

At time "D", the test procedure has been completed, and we wish to return to normal condi-tions. Therefore, the TRCOD pin of the originating NIU is brought high, the originating NIU begins to transmit the loopback reset code, and the responding NIU begins its 4.75 second countdown.

Note that the responding NIU is still in a loopback state, so the reset code is echoed back to the originating NIU. This causes the originating NIU to begin its own 4.75 second countdown as well. Shortly after time "D", RRCOD of the responding NIU goes high, and very shortly after that the RRCOD of the originating NIU goes high. Although we had concerns about the originating NIU reacting to an echoed loopback set code, there are no problems with it reacting to the reset code.

At time "E", about 4.75 seconds after time "D", the responding NIU finishes its countdown and returns to normal service. Once the responding NIU has left the loopback state, the originating NIU may resume normal operations itself. If desired, the circuit shown in Figure 9 could be extended to also monitor the RRCOD output of the originating NIU to determine when the responding NIU has returned to normal opera-tions.

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TEST SCHEME TIMING DIAGRAM Figure 8

NIU "A" – ORIGINATOR

TPOS TNEG	QRSS TEST PATTERN
TSCOD	
TRCOD	
TXTIP TXRING	LOOPBACK SET CODE (00001...) / QRSS TEST PATTERN / LOOPBACK RESET CODE (001...)
RXTIP RXRING	SET CODE / QRSS TEST PATTERN / RESET CODE
RSCOD	
RRCOD REMLB	
RPOS RNEG	SET CODE / QRSS TEST PATTERN / RESET CODE

NIU "B" – RESPONDER

TPOS TNEG	
TSCOD	
TRCOD	
TXTIP TXRING	SET CODE / QRSS TEST PATTERN / RESET CODE
RXTIP RXRING	LOOPBACK SET CODE (00001...) / QRSS TEST PATTERN / LOOPBACK RESET CODE (001...)
RSCOD	
RRCOD	
REMLB	
RPOS RNEG	LOOPBACK SET CODE (00001...) / QRSS TEST PATTERN / LOOPBACK RESET CODE (001...)

A   B   C   D   E

TRANSMITTING A SET CODE Figure 9
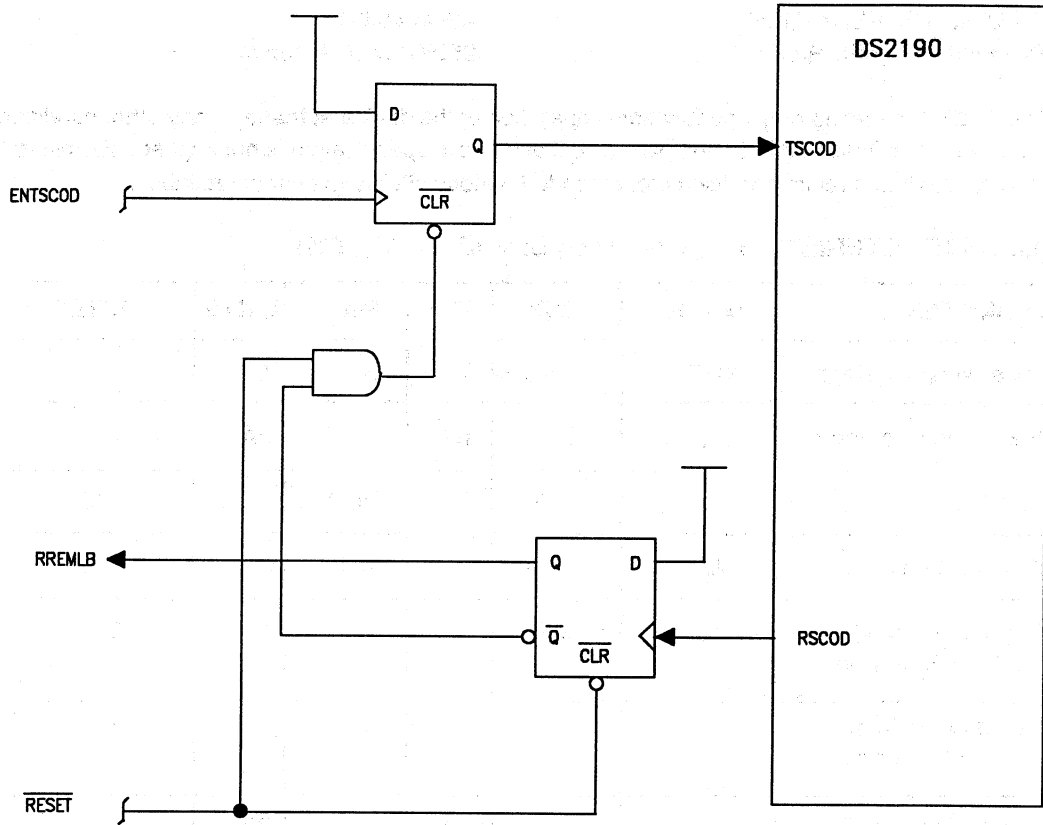
ABSOLUTE MAXIMUM RATINGS

VOLTAGE ON ANY PIN RELATIVE TO GROUND   -0.3V to +7V
OPERATING TEMPERATURE   0 to 70°C
STORAGE TEMPERATURE   -25 to +85°C
SOLDERING TEMPERATURE   260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

D.C. CHARACTERISTICS (T_A = 0-70 deg C; VDD = +5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power supply voltage	VDD	4.75	5.0	5.25	V	
Power supply current	I_{DD}		100		mA	2
Input logic 1 voltage	V_{IH}	2.0		VDD+.3	V	1, 3
Input logic 0 voltage	V_{IL}	-0.3		0.8	V	1, 3
Output high voltage @I_{OH}=-1mA	V_{OH}	2.4			V	1
Output low voltage @I_{OL}=4 mA	V_{OL}			0.4	V	1
Input leakage current $0V \leq V_{IN} \leq V_{DD}$	I_{IL}		0.1	1.0	mA	1

NOTES:
1. D.C. characteristics apply to all customer side pins except LB01 to LB06.
2. I_{DD} specified driving all "ones" into 6000 ft. of 22 AWG cable (worst case).
3. Not applicable to TCLK which is a Schmitt-triggered input.

A.C. DIGITAL CHARACTERISTICS - TRANSMIT (T$_A$=0 to 70°C; VDD = +5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Transmit Data Setup	t$_{TDS}$	50			ns	
Transmit Data Hold	t$_{TDH}$	50			ns	
Frame Sync Setup	t$_{FSS}$	-125		+125	ns	
Frame Sync Width	t$_{FSW}$	100			ns	
Output Delay	t$_{TOD}$			75	ns	
Transmit Clock Frequency	1/t$_{TCW}$	-50ppm	1.544	+50ppm	MHz	1
Transmit Clock High Time	t$_{TCH}$	-1%	324	+1%	ns	1
Transmit Clock Rise Time	t$_{TCR}$			10	ns	2
Transmit Clock Fall Time	t$_{TCF}$			10	ns	2

NOTES:
1. Required to meet PUB 62411 and FCC Part 68 specifications.
2. Measurements made at 1.5V unless otherwise specified.
3. Measured with 10 ns rise and fall times, 100 pF output load unless otherwise specified.

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A.C. DIGITAL CHARACTERISTICS - RECEIVE (T_A=0 to 70°C; VDD = +5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Receive Data Delay	t_{RDD}			75	ns	
Output Delay	t_{ROD}			100	ns	
Receive Clock Frequency	$1/t_{RCW}$		1.544		MHz	
Receive Clock High Time	t_{RCH}	314	324	334	ns	
Receive Clock Low Time	t_{RCL}	314	324	334	ns	
Receive Clock Rise Time	t_{RCR}			20	ns	
Receive Clock Fall Time	t_{RCF}			20	ns	

A.C. DIGITAL CHARACTERISTICS - REMOTE LOOPBACK
(T_A = 0 to 70°C, V_{DD} =5V±5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Code Valid Recognition	t_{RLBCV}		680		ms	1
Code Invalid Recognition	t_{RLBCX}			200	ms	
Remote Loopback State Change	t_{RLB}		4750		ms	1,2
Remote Loopback Reset Delay	t_{RLBRD}			100	ns	
Remote Loopback Reset Pulse Width	t_{RLBPW}	100			ns	

NOTES:
1. Actual time will be within 1% of typical.
2. With REMLB low.

A.C. DIGITAL CHARACTERISTICS - TZERO (t_A = 0 to 70°C, V_{DD} = 5V $\pm$ 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TZERO Valid Delay	t_{TZV}		150		ms	1,2
TZERO Invalid Delay	t_{TZX}			4	us	

NOTES:
1. Actual time will be within 1% of typical.
2. Transmit waveform will meet pulse density requirements if INHDEN is strapped low.

NETWORK INTERFACE CHARACTERISTICS (t_A = 0 to 70°C, V_{DD} = +5V $\pm$ 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
A.C. receive, transmit impedance	Z_R, Z_T		100		ohms	
Receive input signal range	V_{IR}	-30		+0	dBSX	1
RCLK output jitter generation	RxJ_0		0.25		Ulpp	2
Longitudinal balance	LBAL	35			dB	
Transmit ones density (over 192 bits)	TXDENS	12			%	3
Transmit signal level (TXTIP,TXRING)	TXLVL		0		dBSX	4
Transmit keep-alive frequence tolerance (about 1.544 MHz)	TXFTOL	-35		+35	ppm	

NOTES:
1. 0 dBSX = 3V peak.
2. RXTIP and RXRING are connected to a QRSS signal with no jitter present.
3. The ones density of the outgoing transmit signal complies with section 5.4.1 of PUB # 62411. For every time window of 8 X (n + 1) bits - where n can equal 1 through 23 - there will be at least "n" ones present. Also there will be no more that 15 zeros in a row. The DS2190 will ensure that input data at TPOS and TNEG meet these requirements by inserting ones at the violation times (only if INHDEN is low).
4. 0 dB of LBO selected.

TRANSMIT A.C. TIMING DIAGRAM Figure 10
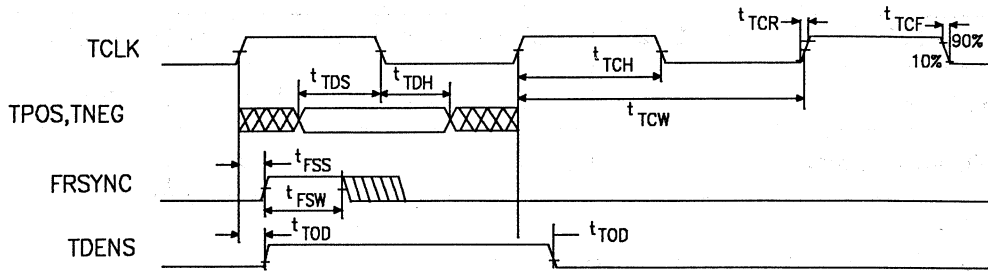
RECEIVE A.C. TIMING DIAGRAM Figure 11
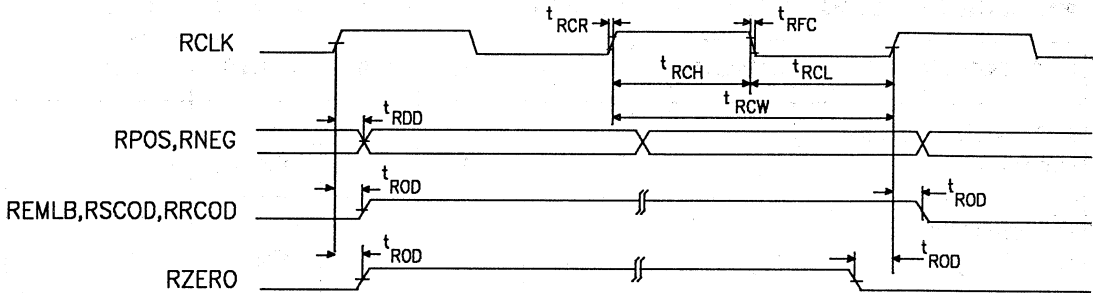
REMOTE LOOPBACK A.C. TIMING DIAGRAM Figure 12
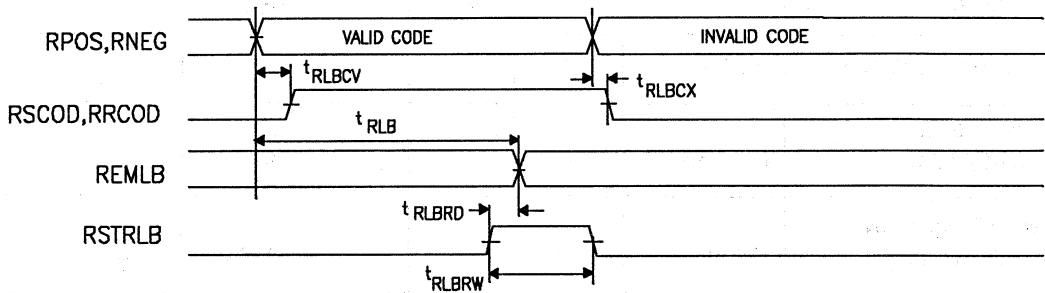
TZERO A.C. TIMING DIAGRAM Figure 13
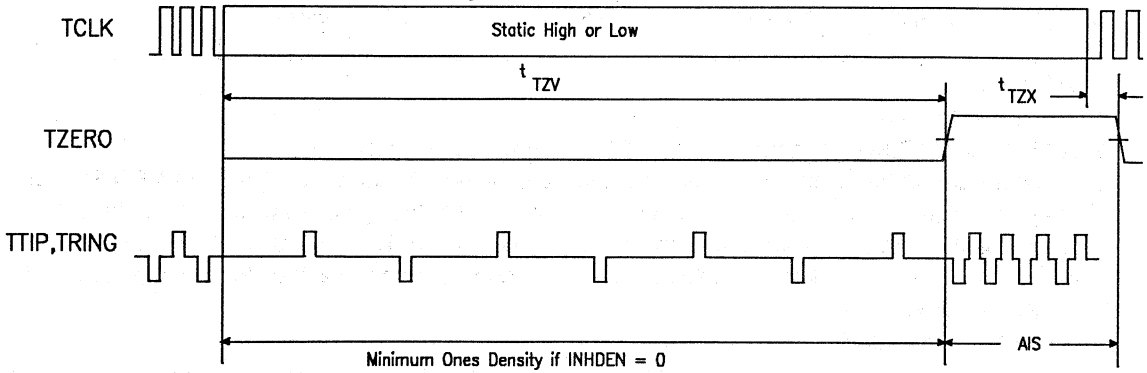
T1 NETWORK INTERFACE UNIT (NIU)
DS2190
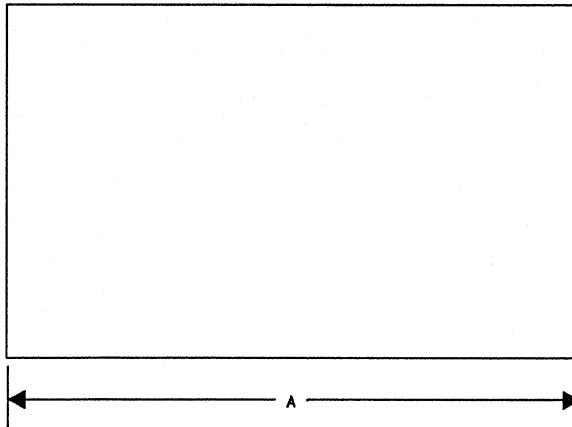
DIM.	INCHES	
	MIN	MAX
A	3.080	3.100
B	1.885	1.905
C	.490	.510
D	.540	.560
E	.070	.090
F	.220	.240
G	.090	.110
H	1.840	1.860
J	.010	.014
K	.018	.022

20 EQUAL SPACES AT
.100 ± .010 TNA

6
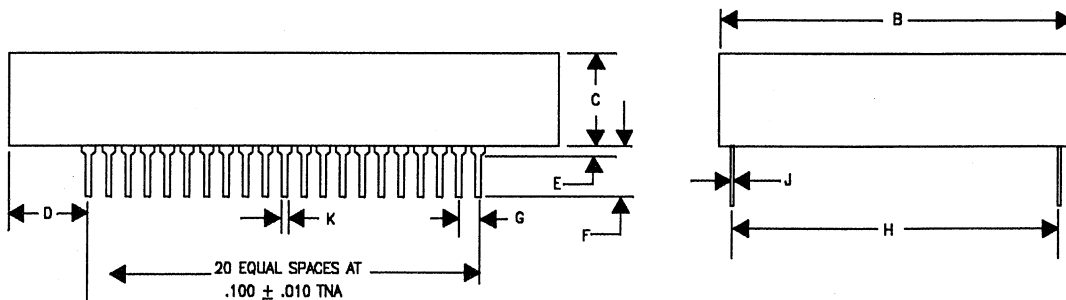
These package dimensions represent prototype packaging. Dimensions B, E, F, J and K are subject to change.

Line Cards

Dallas Semiconductor
T1/CEPT LINE CARD
SipStik

FEATURES
• Complete T1 or CEPT line card

• Performs the following functions:
  - line interface
  - framing
  - monitoring
  - buffering

• Includes transformers, line terminations, and capacitors

• Interfaces directly to transmit and receive twisted wire pair or coax

• Local and line loopback capability

• Separate analog and digital grounds and supplies for increased analog performance

• Conforms to JEDEC SIMM standard

• Simple serial interface port for use with microprocessor; used to control the card and monitor status of the line and the incoming data

• Fully CMOS for low power consumption

• Can operate off a single +5V supply

DESCRIPTION
The DS2280 and DS2281 implement a complete line card function on a single 0.85" x 3.85" SIMM card. The DS2280 complies to the T1 standard (DSX-1 interface) while the DS2281 complies to the CEPT standard (0 to -6dB interface). For

COMPONENT PLACEMENT
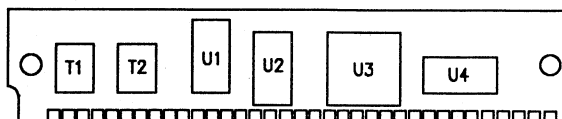
U1	- DS2186	
U2	- DS2187	
U3	- DS2180A (for DS2280) or DS2181 (for DS2281)	
U4	- DS2175	

more component information, see the data sheets on the DS2180A, DS2181, DS2175, DS2186 and DS2187. To obtain detailed product information, contact your local sales office.

Modems

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Dallas Semiconductor
MODEM

DS6101/6103

FEATURES

- Direct connection to telephone line —
  incorporates DAA function
- Parallel interface to general purpose uP bus
- Very small size — 2.28" x 1.0" x 0.5"
- Full Bell 212A/103 Modem compatibility
- FCC Part 68 registered DAA
- Call progress Monitoring
- Tone or pulse dialing
- DTMF sensing and decoding
- Voice sensing
- Software controlled audio interface
- Voice synthesis option
- Parallel host interface
- +/- 5 Volt power only
- Telephone line diagnostics
- Synchronous/asynchronous operation
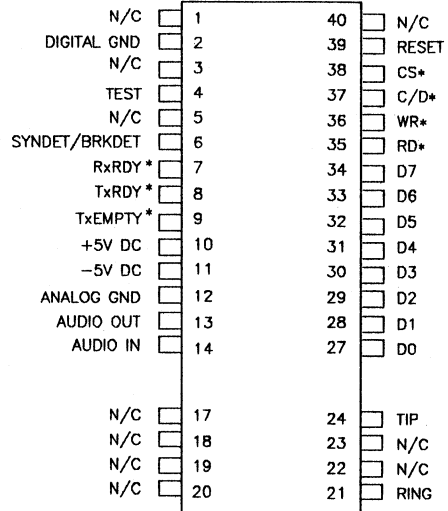- Line frequency monitoring
- Parity generation/checking
- Sync byte detection/insertion

PIN CONNECTION

```
         N/C   [ 1        40 ]  N/C
   DIGITAL GND [ 2        39 ]  RESET
         N/C   [ 3        38 ]  CS*
        TEST   [ 4        37 ]  C/D*
         N/C   [ 5        36 ]  WR*
SYNDET/BRKDET  [ 6        35 ]  RD*
      RxRDY *  [ 7        34 ]  D7
      TxRDY *  [ 8        33 ]  D6
     TxEMPTY * [ 9        32 ]  D5
      +5V DC   [ 10       31 ]  D4
      -5V DC   [ 11       30 ]  D3
   ANALOG GND  [ 12       29 ]  D2
    AUDIO OUT  [ 13       28 ]  D1
     AUDIO IN  [ 14       27 ]  D0

         N/C   [ 17       24 ]  TIP
         N/C   [ 18       23 ]  N/C
         N/C   [ 19       22 ]  N/C
         N/C   [ 20       21 ]  RING
```

CAUTION
Pins 17-24 have 1500V isolation from the rest of the modem, this isolation should be preserved throughout the system.

DESCRIPTION
The DS6101/6103 Modems are high level communication subsystems manufactured in a component sized form factor to enable maximum communications capability in a minimum amount of space. The distinguishing characteristic of these devices is that they allow direct connection to a telephone line from any general purpose microprocessor bus. In contrast to many of the so-called "single-chip modem" IC's, the DS6101/6103 Modems provide all of the functions required for a complete, Bell 212A compatible interface. These functions include the host interface, modulation and demodulation circuitry, and Data Access Arrangement (DAA) line interface ciruitry. The Modems' DAA is fully FCC registered, eliminating potential delays for customers with a need to incorporate a modem function in their end system product.

The Modem has an advanced line monitoring capability which allows it to sense the presence of voice or DTMF (touch tone) signals on the line in addition to its normal call progress monitoring. The Modem may then be switched into an Audio mode for voice communication, or into a DTMF decoding mode which makes it possible to receive information from a remote touch tone telephone and decode it for the host processor. The DS6103 includes a voice synthesizer for voice prompting in the return path or for the user.

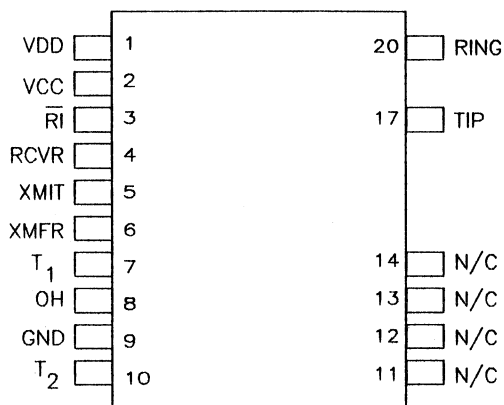For more information on this product, see the Modem Designers Guide.

DAA

Dallas Semiconductor
Data Access Arrangement

DS6112

FEATURES

- Interfaces user equipment to public switched telephone network

- FCC Part 68 Registered
  - Simplifies system design
  - Minimizes equipment approval cycle

- Ideal for modem applications

- Small Size - 1.25" x 1.0" x 0.5"

- 2 to 4 Wire Converter

- 1500 Volt Isolation

- 800 Volt Surge Protection

- Ring Detection

PIN CONNECTIONS

Pin	Name		Pin	Name
1	VDD		20	RING
2	VCC		17	TIP
3	$\overline{RI}$			
4	RCVR			
5	XMIT			
6	XMFR			
7	T_1		14	N/C
8	OH		13	N/C
9	GND		12	N/C
10	T_2		11	N/C

CAUTION
Pins 17 and 20 have 1500V isolation from the rest of the circuitry. This isolation should be preserved throughout the system.

DESCRIPTION

The DS6112 is a communications component that provides a "direct connect" telephone line interface. It is FCC Part 68 Type WP registered to meet hazardous voltage, surge and leakage current requirements. A system developed with this product as the DAA meets Part 68 Type WP protection requirements and requires no further registration.

This component may be used as the direct connect telephone line interface for virtually any application in which voice or data is to be transmitted over the public switched telephone network.

The DS6112 includes both ring detection circuitry and the 2 to 4 wire converter hybrid for use in modem applications. It operates from +/-5 volt power supplies and occupies 1.25 square inches of board space.

For more information on this product, see the Modem Designers Guide.

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Dallas Semiconductor
ADPCM DESIGN KIT

FEATURES

- Emulates multi-channel applications such as T1 transcoders

- Expedites new designs by eliminating first-pass device prototyping

- Interfaces directly to IBM PC, XT, AT and compatibles

- High-level, graphic software demonstrates chip flexibility and feature set

- Kit components include:

  - DS2167 ADPCM processors (2)

  - Codec-combo devices (2)

  - Timeslot assigner circuit (TSAC) for combos

  - Support logic and clock generation circuitry

  - Printed circuit board

  - Interface cable for PC

  - Documentation and control software diskette
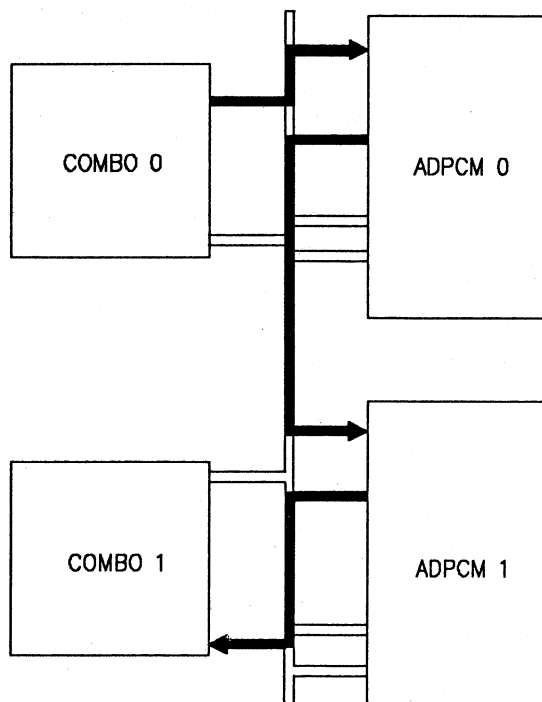
DESCRIPTION

The ADPCM design kit provides everything a user needs to evaluate the DS2167 (DS2167K) ADPCM processors in an actual system environment. The evaluation board connects directly to transmission test sets for performance monitoring of compressed or expanded channels. The board requires ±5 volts. A system control interface connects directly to the PC parallel printer port.

The kit's control software turns the PC into a powerful system controller. The program gives the user full control of system configuration, including timeslot placement, operating modes (comprossion, expansion, bypass or idle), data formats and algorithm reset. The controller program runs under MSDOS or IBM DOS version 2.0 or later. Color monitors are supported but not required.

1. INTRODUCTION

The DS2167 Evaluation Kit simplifies system level evaluation of the Dallas Semiconductor DS2167 ADPCM Processor. The DS2167 is a single CMOS integrated circuit which implements the recommended T1Y1 ADPCM 32K-bit speech compression/expansion algorithms for two independent channels. Not only does the DS2167 contain a high-speed DSP engine optimized for the ADPCM algorithms, but it also contains on-chip control and timing circuitry to minimize support logic for connection to serial PCM backplanes. A microcontroller compatible interface allows the DS2167 configuration to be defined by an external microcontroller. This kit allows performance evaluation of multiple-channel ADPCM processing systems. The kit includes an evaluation board and controller software.

The DS2168 Evaluation Kit is identical to the DS2167 Evaluation Kit, except that DS2168 ADPCM Processors are substituted for the DS2167. This device implements the older CCITT ADPCM algorithm. Except where noted, all information equally applies to both kits.

1.1 The Evaluation Board

The evaluation board is a self-contained, multi-channel speech compression/expansion system. A block diagram of the DS2167 Evaluation Board is shown in Figure 1. It contains two DS2167 ADPCM Processors and two CODEC/filter combos, all connected by a common PCM highway.

DS2167 access to the highway is controlled by on-chip channel time slot counters; combo access is controlled by a separate time slot assignment circuit (TSAC). A 1.544MHz data clock (BCLK) and 8KHz frame synchronization clock (SYNC) are generated on the Evaluation Board and routed to all synchronous elements. Four BNC connectors allow connections to the analog inputs and outputs of the two combos. Power-on reset for the DS2167s is provided by a DS1232 Micromonitor.

The board contains a configuration control port which connects directly to the parallel (printer) port of an IBM PC/XT/AT or compatible personal computer. If the computer has multiple printer

DS2167 EVALUATION BOARD BLOCK DIAGRAM Figure 1

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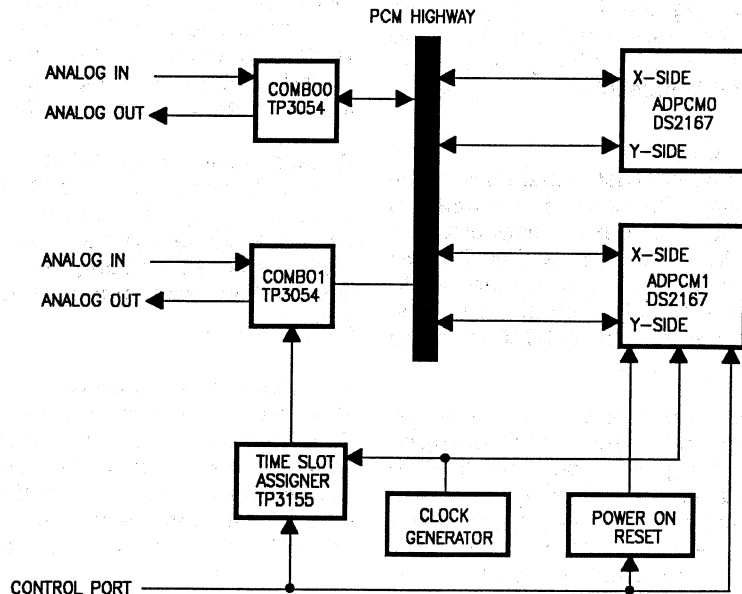
ports, the evaluation board may be connected without interfering with normal printer operation.

Section two of this manual describes the evaluation board.

1.2 The Controller Software
The provided controller software turns an IBM PC (or compatible computer) into a system controller for the evaluation board. The program communicates with the evaluation board through a parallel (printer) port. The controller displays a system configuration. First, the user makes any configuration changes he or she desires. The display will be updated to reflect these changes. When all the changes have been made, the user directs the controller program to write the displayed configuration to the evaluation board.

The controller software runs under MSDOS or IBM DOS. It takes advantage of color monitors (both standard CGA and EGA color video adapters), but monochrome adapters may also be used. Several predefined configuration data files are included as examples. Section three of this manual describes the controller software, including setup instructions.

2. THE EVALUATION BOARD
This section discusses the DS2167 Evaluation Board hardware. First, the data paths through the board, including the PCM highway, are reviewed. Next the miscellaneous clocking and reset circuits are discussed. Finally, the configuration control port is presented.

2.1 The PCM Highway
All PCM data and ADPCM data travel along a common PCM highway. The combos and DS2167s are assigned time slots to place data onto and take data away from the highway. The DS2167 accomplishes this function with no external circuitry—it contains on-chip time slot counters. The combos require an external TSAC to control highway access.

Each combo has a pair of BNC connectors—one for its analog input and one for its analog output. The input signal is converted to PCM data and placed onto the highway during the combo's transmit time slot. The output signal is generated from the PCM data on the highway during the combo's receive time slot.

Data on the highway is grouped into frames of 193 bits. One bit occurs during the frame sync—the remaining 192 bits are divided into time slots. For PCM data, there are 24 8-bit time slots numbered 0 through 23. For ADPCM data, there are 48 4-bit time slots numbered 0 through 47. Time slot assignments are illustrated in figure two. Note that PCM and ADPCM data is carried over the same bus. Therefore it is undesirable, for example, to have one device transmitting PCM data during time slot 2 and another transmitting ADPCM data during time slot 5.

Each combo is assigned two time slots—one for transmit data and one for receive data. Each DS2167 is assigned four time slots—a transmit/receive pair for the X-side and another pair for the Y-side. Time slot values range from 0 to 63. Note that a device can be assigned a time slot which does not occur, which effectively disables the device. This is because the frame sync signal resets the TSAC and DS2167 time slot counters to zero, and the frame sync occurs after time slot 23. For example, if a combo is assigned a transmit time slot greater than 23, then the combo will never transmit data.

2.2 Clocking and Reset Circuitry
The DS2167 Evaluation Board contains a 1.544MHz data clock (BLCK) which runs to all synchronous elements. This clock is divided by 193 to obtain an 8KHz frame sync (SYNC) which is connected to both DS2167s and the TSAC. The TSAC generates the sync pulses which control combo processing. The TSAC supplied with the evaluation kit is the TP3155.

Power on reset for the DS2167s is provided by a DS1232 Micromonitor. The DS2167s may also be reset through the control port. The TSAC powers up with all sync pulses inhibited. A sync pulse is enabled (and only that sync pulse is enabled) when programmed through the control port.

2.3 Configuration Control
This section describes how the Evaluation Board control port works. It provides sufficient detail to construct controller hardware and software for the board. Note that the provided software alleviates the need to know these details, so most users may skip this section.

TIME SLOT ASSIGNMENTS Figure 2

```
                        PCM TIME SLOTS
                              ⁄⁄
  ┌─┬──────┬──────┬──────┬─┐ ⁄ ┌──────┬──────┐
  │F│  0   │  1   │  2   │ │ │ │  22  │  23  │
  └─┴──────┴──────┴──────┴─┘ ⁄ └──────┴──────┘
                            ⁄⁄

  ◄─────────────────── 125 usec ───────────────────►

  ┌─┬───┬───┬───┬───┬───┬───┬─┐ ⁄ ┌────┬────┬────┬────┐
  │F│ 0 │ 1 │ 2 │ 3 │ 4 │ 5 │ │ │ │ 44 │ 45 │ 46 │ 47 │
  └─┴───┴───┴───┴───┴───┴───┴─┘ ⁄ └────┴────┴────┴────┘
                               ⁄⁄
                      ADPCM TIME SLOTS
```
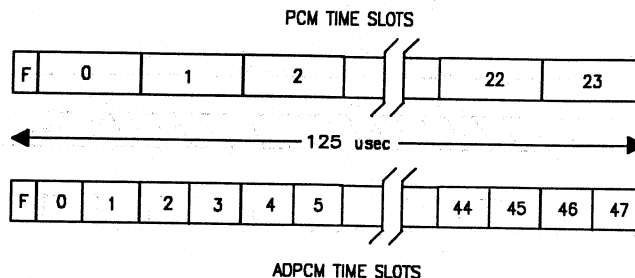
The DS2167 contains a serial port which allows an external controller to define the device configuration. The configuration parameters include the input (receive) time slot, the output (transmit) time slot, the data format (u-Law or A-Law), the device mode (compress, expand, 4-bit bypass, 8-bit bypass, or idle), and algorithm reset control. This information is defined independently for the X and Y channels. Please refer to the DS2167 data sheet for information on these parameters and the serial port interface protocol.

The TSAC generates the sync pulses which control the combo's transmit and receive time slots. It contains a serial port for specifying time slot numbers and three control lines (CH0, CH1, and CH2) for associating the time slot number with a specific sync signal. Serial data is driven on the DC line and latched on the falling edge of the CLKC line. The configuration sequence is enabled by driving the CS line low. The protocol for the TSAC is shown in Figure 3. The T5 through T0 bits specify the time slot number. The X and R bits are both high to disable the associated channel (by suppressing that channel's sync pulse); any other value enables the sync pulse. Please refer to the TP3155 data sheet for further information.

The user can access both the DS2167 and TSAC through the Evaluation Board's control port. Figure 4 shows the connector pin assign-

ments. For reference, the table shows the standard PC parallel port signal designations along with the Evaluation Board signal definitions. The input/output information is specified with respect to the DS2167 Evaluation Board.

The various signals are used as follows:

2.3.1 SCLK The serial data clocking signal for both the DS2167s and the TSAC. Note that the DS2167 latches serial data on the rising clock edge, while the TSAC latches data on the falling edge.

2.3.2 SDATA The serial data for both the DS2167s and the TSAC. Note that the DS2167 data bytes are written to the port least significant bit first, while TSAC data is written most significant bit first.

2.3.3 CSADPCM/ Chip select for both DS2167s. This signal should be low when either DS2167 serial port is being written, otherwise it should remain high.

2.3.4 CSTSAC/ Chip select for the TSAC. This signal should be low when the TSAC serial port is being written, otherwise it should remain high.

2.3.5 TSACCHAN This signal specifies the combo for which the time slot assignment is being made; it is the TSAC's "CH0" input. It should

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TSAC CONTROL INTERFACE Figure 3
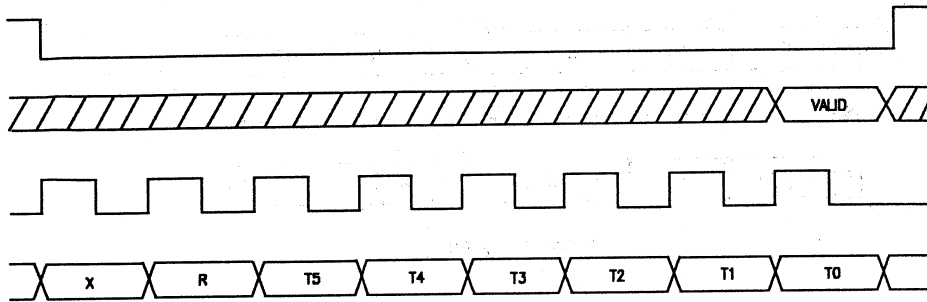
CONTROL PORT CONNECTIONS Figure 4

Header Pin	Signal Dir.	Board Signal	Port Signal	DB-25 Pin
1	input	SCLK	STROBE/	1
3	input	SDATA	BIT0	2
5	input	CSADPCM/	BIT1	3
7	input	CSTSAC/	BIT2	4
9	input	TSACCHAN	BIT3	5
11	input	TSACSIDE	BIT4	6
13	input	- -	BIT5	7
15	input	- -	BIT6	8
17	input	- -	BIT7	9
19	output	wired low	ACK/	10
21	output	wired low	BUSY	11
23	output	wired low	PEND	12
25	output	wired high	SELECT	13
2	input	- -	AUTOFEED/	14
4	output	wired high	ERROR/	15
6	input	RESET/	INIT/	16
8	input	- -	SELINP/	17
10-24	- -	ground	ground	18-25
26	- -	no connect	- -	- -

be low when assigning a combo 0 time slot and high when assigning a combo 1 time slot. It is latched by the TSAC at the same time as the T0 serial data bit.

2.3.6 TSACSIDE This signal specifies whether the time slot assignment is for a combo transmit or receive side; it is the TSAC's "CH2" input. It should be low when assigning a transmit time slot and high when assigning a receive time slot. It is latched by the TSAC at the same time as the "T0" serial data bit.

2.3.7 RESET/ Active low signal which generates a reset for the DS2167s. Please refer to the DS1232 Micromonitor data sheet for details on the timing of the reset signals.

2.3.8 Outputs The five output pins are hardwired to form a board "signature." This signature may be used to determine if the board is present on a particular printer port. If the board is connected to a PC with the provided cable, the signature may be checked by reading the parallel adapter's STATUS port and looking for a binary pattern "10011XXX."

3. CONTROLLER SOFTWARE

The DS2167 Evaluation Board Controller program allows the user to control the Evaluation Board configuration. A high level, graphic interface simplifies this task. In addition, several "canned configuration" data files are included to demonstrate some different board configurations.

3.1 Requirements and Setup

The ADPCM.EXE controller program is shipped on a DOS-compatible floppy disk. The program will run under MSDOS or IBM DOS on an IBM/PC, IBM/AT, or compatible personal computer. While the program takes advantage of color graphics, a monochrome display adapter may be used. A parallel printer port must be available on the PC for connecting the evaluation board. The procedure is as follows:

1. Make sure that the controller program can be accessed by either copying "ADPCM.EXE" from the floppy disk to the hard disk, or place the floppy disk in the drive and make that drive the current drive.

2. Connect the evaluation board to any parallel printer port on the PC with the provided

interface cable.

3. Connect transmission test set or other equipment to the evaluation board's BNC connectors.

4. Connect power (+5 volts, -5 volts, ground) to the evaluation board, and turn the power supply on.

5. Start the controller program by typing "ADPCM".

NOTE—It is important that the board is powered up before the controller program is started. This is so that the program can find the board.

When the program is invoked, it automatically determines your system configuration. Specifically, it determines whether you are using a color monitor or a monochrome monitor, and it determines if the Evaluation Board is connected to the LPT1 or LPT2 port (or not connected at all).

3.2 Screen Display

When invoked, a representation of the Evaluation Board configuration is drawn on the screen. This configuration may be edited and then written to the Evaluation Board. Figure 5 shows an example screen display. The following discussion will frequently reference this example to illustrate how the program works. The display shows four devices connected to the highway: COMBO0, COMBO1, ADPCM0, and ADPCM1. These represent the two combos and DS2167s, respectively.

In the following discussion, the terms *connection* and *link* will be used. A connection is any point which may access the highway, such as the ADPCM0 XIN pin. There are twelve possible connections on the Evaluation Board. A link consists of one or more connections which access the highway at the same time, either transmitting data or receiving data.

3.2.1 Time Slots The controller program shows connections at the combos and DS2167s leading to the PCM highway. Next to each connection is the time slot number associated with that connection. For example, figure five shows that COMBO0 will transmit during time slot 1 and receive during time slot 2.

CONTROLLER DISPLAY EXAMPLE Figure 5

```
┌─────────────────────────┐                    ┌──────────────────────────────────────┐
│                    1 DX │━━━━━━━━━━━┓         │ XIN    1                    COMPRESS │
│   COMBO 0               │           ┃         │ XOUT   10 [5]                  u-LAW │
│                    2 DR │           ┃         │ ─────────────── ADPCM 0 ──────────── │
└─────────────────────────┘           ┃         │ YIN    10[5]                  EXPAND │
                                      ┃         │ YOUT   2                       u-LAW │
┌─────────────────────────┐           ┃         └──────────────────────────────────────┘
│        STATUS           │           ┃
│   Not written to board  │           ┃         ┌──────────────────────────────────────┐
│                         │           ┃         │ XIN    0                        IDLE │
└─────────────────────────┘           ┃         │ XOUT   0                       u-LAW │
                                      ┃         │ ─────────────── ADPCM 1 ──────────── │
┌─────────────────────────┐           ┃         │ YIN    0                        IDLE │
│                   23 DX │           ┃         │ YOUT   0                       u-LAW │
│   COMBO 1               │           ┃         └──────────────────────────────────────┘
│                   23 DR │           ┃
└─────────────────────────┘
```
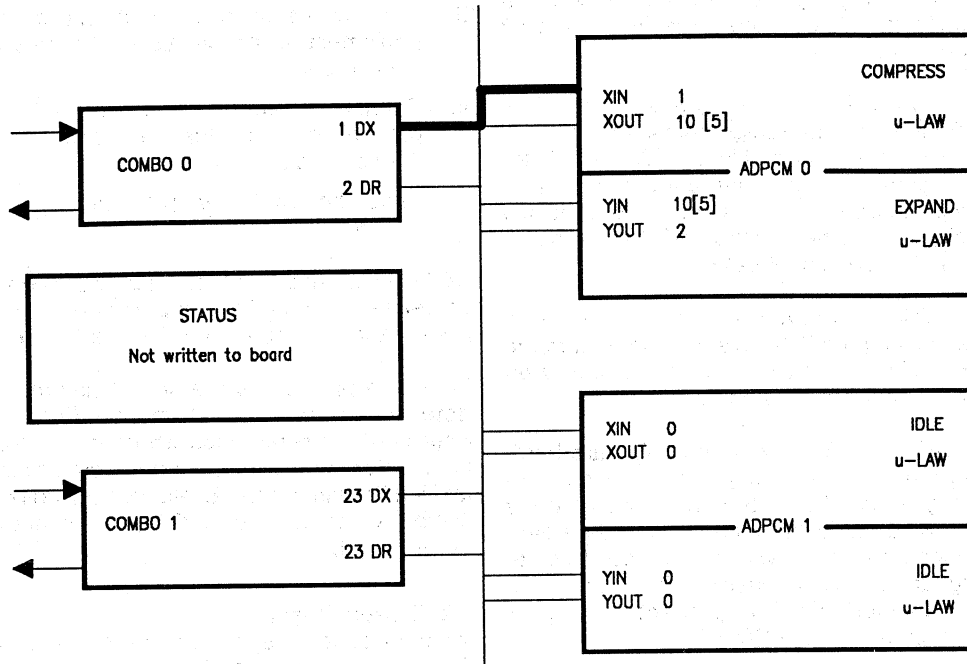
Recall that 8-bit PCM and 4-bit ADPCM use different time slot numbering conventions, but they are transmitted together on the highway. For this reason, any connection which is transmitting or receiving ADPCM shows a number in brackets next to the time slot number. This bracketed number is the 8-bit PCM time slot which occurs at the same time as the programmed 4-bit time slot. The example shows that ADPCM0 will be transmitting 4-bit data on XOUT during time slot 10. ADPCM time slot 10 occurs at the same time as PCM time slot 5, so "5" is shown in brackets.

3.2.3 Formats and Modes The data format and operating mode of the DS2167s are also shown. The two possible data formats are *A-Law* and *u-Law*. The X-side of ADPCM0 is processing *u*-Law data in the example. The possible operating modes are *compress, expand, bypass-4, bypass-8,* and *idle*. The X-side of ADPCM0 is compressing 8-bit PCM data to 4-bit ADPCM data in the example.

The mode and format may be programmed only for the DS2167s—the combos are fixed. The combos shipped with the DS2167 Evaluation Kit process *u*-Law data, which is why the DS2167s are initially defined to *u*-Law format. If desired, you may replace the combos with TP3057 A-Law combos and reconfigure the DS2167s for A-Law data.

3.2.3 Connection Selection One connection on the screen is always considered the "selected connection." The selected connection is indicated by a highlighted time slot number. In the example it is the transmit connection of COMBO0, and if any configuration changes are made they will affect this connection. A different connection is selected with the cursor movement keys.

3.2.4 Links The link containing the selected connection is highlighted. This makes it easy to follow data flow through the Evaluation Board. The example shows that a link exists between

the COMBO0 DX connection and the ADPCM0 XIN connection. That is because the former is transmitting data during time slot 1 and the latter is receiving data during the same time slot. If the COMBO0 DX time slot was changed, then there would no longer be a link between it and ADPCM0 XIN, so the highlighted link would be removed. If the new transmit time slot linked COMBO0 to another device, then the new link would be highlighted.

Sometimes there can be problems in the links—you can create conflicting connections or mismatched connections. Conflicting connections occur when two connections try to transmit data onto the highway at the same time creating bus contention. Mismatched connections occur when two connections access the highway at the same time, but access it for different types of data. For example, if one device transmits PCM data and another device picks up half of it as ADPCM data, then these connections are mismatched.

When a color display is used, normal links are shown in blue, conflicting connections are shown in red, and mismatched connections are shown in pink (magenta). When a monochrome display is used, normal links are emboldened, conflicting connections blink in bold intensity, and mismatched connections blink in normal intensity. Even though the controller program locates problems between connections, the user is still free to program any configuration he or she desires.

3.2.5 Status Messages
The "status" box may contain one of the following status messages:

- board not present
- not written to board

The "board not present" message indicates that the program doesn't see a DS2167 Evaluation Board connected to a parallel port. If the program can't find a board, then it will disable the commands which talk to the board. If you receive this message, verify that the evaluation board is properly connected to the PC and it is powered up. You can also verify the system configuration with the "F2" setup command discussed shortly.

The "not written to board" message indicates that the configuration shown on the screen has not been written to the Evaluation Board. The configuration is only written upon request from the user. This message will be displayed when the program first starts (unless no board is present), and any time changes are made. This message is removed when the configuration is written to the Evaluation Board.

3.3 Connection Selection Commands
As mentioned, configuration commands only affect the selected connection—which is indicated by a highlighted time slot number. The cursor movement keys may be used to select a different connection. The recognized keys are:

- cursor up
- cursor down
- cursor left
- cursor right
- home
- end
- page up
- page down

The first four keys work much as expected—they move in the indicated direction. In the example, pressing the "cursor down" key will select the COMBO0 DR connection. In this case, the time slot value of "2" would be highlighted, and the link to ADPCM0 YOUT would be highlighted. Moving off the end of the screen wraps around to the other side. In the example, pressing the "cursor up" key will select the COMBO1 DR connection.

The "home" key moves to the top-left connection on the screen (COMBO0 DX). The "end" key moves to the bottom-right connection on the screen (ADPCM1 YOUT).

The last two cursor movement keys provide ways of quickly accessing other connections in a link. The "page up" key moves up the screen to the next connection which is linked to the selected connection. If there are no other connections linked to the selected connection then no changes are made. The "page down" key works similarly but it moves down the screen to the next connection in the link.

3.4 Keyboard Entry
Many of the remaining commands require keyboard entry from the user (e.g. a file name, a device mode, etc.). As the user types, the characters are displayed at the

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bottom of the screen. Editing is performed with the "backspace" key (delete last character) and the "escape" or "control/U" keys (delete line).

3.5 Configuration Commands Once a connection has been selected (with the aforementioned cursor movement keys), several commands are available for changing that device's configuration, specifically the time slot, data format, and operating mode. Press the "ENTER" key after the command is typed. Commands may be in either upper case or lower case. Only the first character of the command is required. For example, "bypass," "BYPASS", "ByPaSs", "b", and "byp" all mean the same thing.

3.5.1 Time Slot Selection When a number between 0 and 63 is entered, the time slot for the selected connection is changed to that number.

3.5.2 Data Format Selection The DS2167s may process either *u*-Law or A-Law data. The data format is specified independently for each side. To change the data format on one side of a DS2167, select either connection on that side and enter one of the following commands:

- *u*-Law
- A-Law

The hyphen need not be typed, so "U-LAW", "ULAW", and "U" all accomplish the same thing.

3.5.3 Operating Mode Selection The ADPCM operating mode is specified by selecting either connection on a side and specifying:

- Compress
- Expand
- Bypass
- Idle

Note that there are two different bypass modes: "bypass-4" which processes 4-bit ADPCM data and "bypass-8" which processes 8-bit PCM data. Each entry of the "bypass" command toggles between these two modes.

3.6 Function Key Commands
Some commands use the special function keys. They include:

F1 - Help
F2 - Change Program Setup
F3 - Write Configuration
F4 - Reset Board
F5 - Reset ADPCM Algorithm
F6 - Change ADPCM Address
F7 - Load from File
F8 - Save to File
F9 - DOS Escape
F10 - Exit Program

Some of these commands require information (such as a file name) to be entered. The user should type in the required information and then press the appropriate function key. The "ENTER" key should not be used.

3.6.1 F1—Help The "F1" help key displays a summary of the controller program commands.

3.6.2 F2—Setup When the controller program is started, it automatically determines the monitor type and where the Evaluation Board is connected. The "F2" key allows you to examine and modify the setup.

3.6.3 F3—Write Configuration Once a board configuration has been entered, the "F3" write configuration key sends the configuration to the board. Note that the board isn't updated as configuration changes are made—the "F3" key must be used to write out the configuration.

3.6.4 F4—Reset Board The "F4" reset key issues a reset to the DS2167s on the Evaluation Board. Once the devices are reset, you will need to use "F3" to program them again. The reset does not affect the combos or TSAC. A reset is automatically performed when the controller program is started.

3.6.5 F5—Reset Algorithm The "F5" key sends an algorithm reset request to the selected ADPCM. This request causes the DS2167 to reset the algorithm coefficients to their initial conditions. Note that this command does not change the device's configuration, and it only affects one side ('X' or 'Y') of a device. For example, if the "ADPCM0 XIN" connection is selected, then "F5" will reset the algorithm registers for the X-side of ADPCM0.

3.6.6 F6—Change Address The ADPCM0 and ADPCM1 pins A0 through A5 are hardwired on the Evaluation Board to addresses 0 and 1 respectively. The controller program normally uses these addresses. If hardware modifications are made to the board, the "F6" change address key may be used to select different device addresses. Use this command by entering a valid ADPCM device address (between 0 and 63) and then press "F6". The first time you try this, the controller program will ask if you want to allow changes to the device addresses. If you answer "Y" (for yes), then the display will be updated to show the ADPCM device address in brackets immediately following the device number. Unless the user modifies the evaluation board, he or she will probably not want to use this command.

3.6.7 F7—Load Configuration The "F7" load configuration command is used to load an evaluation board configuration from a file. This might be one of the "canned configuration" files included with the ADPCM Evaluation Kit, or a file created with the "F8" save configuration command. To use this command, enter a file name and then press "F7". Be sure that you enter the full file name. For example, if you want to load the "FULLDUP.DAT" file, then specify that, not just "FULLDUP". This command does not actually change the board configuration—you will need to use the "F3" write configuration key to do that.

3.6.8 F8—Save Configuration The "F8" save configuration command is used to save the configuration shown on the screen to a file. This configuration may be recalled at a later time with the "F7" load configuration command. To use this command, enter a file name and then press "F8".

3.6.9 F9—DOS Escape The "F9" key allows access to DOS without terminating the controller program. If a command is typed (e.g. "dir") and then "F9" is pressed, then that command will be run. If no command is typed, then pressing "F9" will pause execution of the controller program and pass control to DOS. When you are ready to return to the controller program, type "exit". In order for "F9" to work properly, you need to ensure that the controller program will be able to find "COMMAND.COM". If "F9" fails

to work properly, ensure that the DOS "COMSPEC" parameter is properly set. If a DOS parameter called "SHELL" is defined then it will be used for DOS escapes instead of "COMMAND.COM" This command does not change the evaluation board status—it will continue to operate while the controller program is suspended.

3.6.10 F10—Exit Program The "F10" key terminates execution of the controller program. Note that exiting the program does not change the evaluation board status—it will continue to operate in the most recently defined configuration.

3.7 Additional Commands Two additional commands are:

- Control/L
- Control/C

"Control/L" redraws the display. "Control/C" terminates the program, and is equivalent to the "F10" function key.

3.8 Canned Configurations Four "canned configurations" are provided with the DS2167 Evaluation Kit. They are stored in the files "INITIAL.DAT", "EXAMPLE.DAT", "COMPARE.DAT" and "FULLDUP.DAT".

The "INITIAL.DAT" file contains the same configuration as when the program is first invoked. This file may be loaded to "start over from the beginning."

The "EXAMPLE.DAT" file contains the configuration shown in Figure 5 which has been used as an example throughout this document.

The "COMPARE.DAT" configuration allows the impact of compression/expansion to be compared. The analog input from COMBO0 is compressed, then expanded, and then output through COMBO0. The COMBO1 output is taken from the COMBO0 input, so the two combo outputs can be compared to see the effects of ADPCM processing. COMBO1 does no transmission in this configuration; only the receive side is used.

The "FULLDUP.DAT" configuration sets up a full duplex connection between the two combos. The input from COMBO0 is compressed, then expanded, and then output through COMBO1.

The COMBO1 input is compressed, expanded, and output through COMBO0.

4. CONCLUSION

The DS2167 Evaluation Kit demonstrates multiple ADPCM Processors operating in a single system. Due to the on-chip time slot counters and serial control port, this is accomp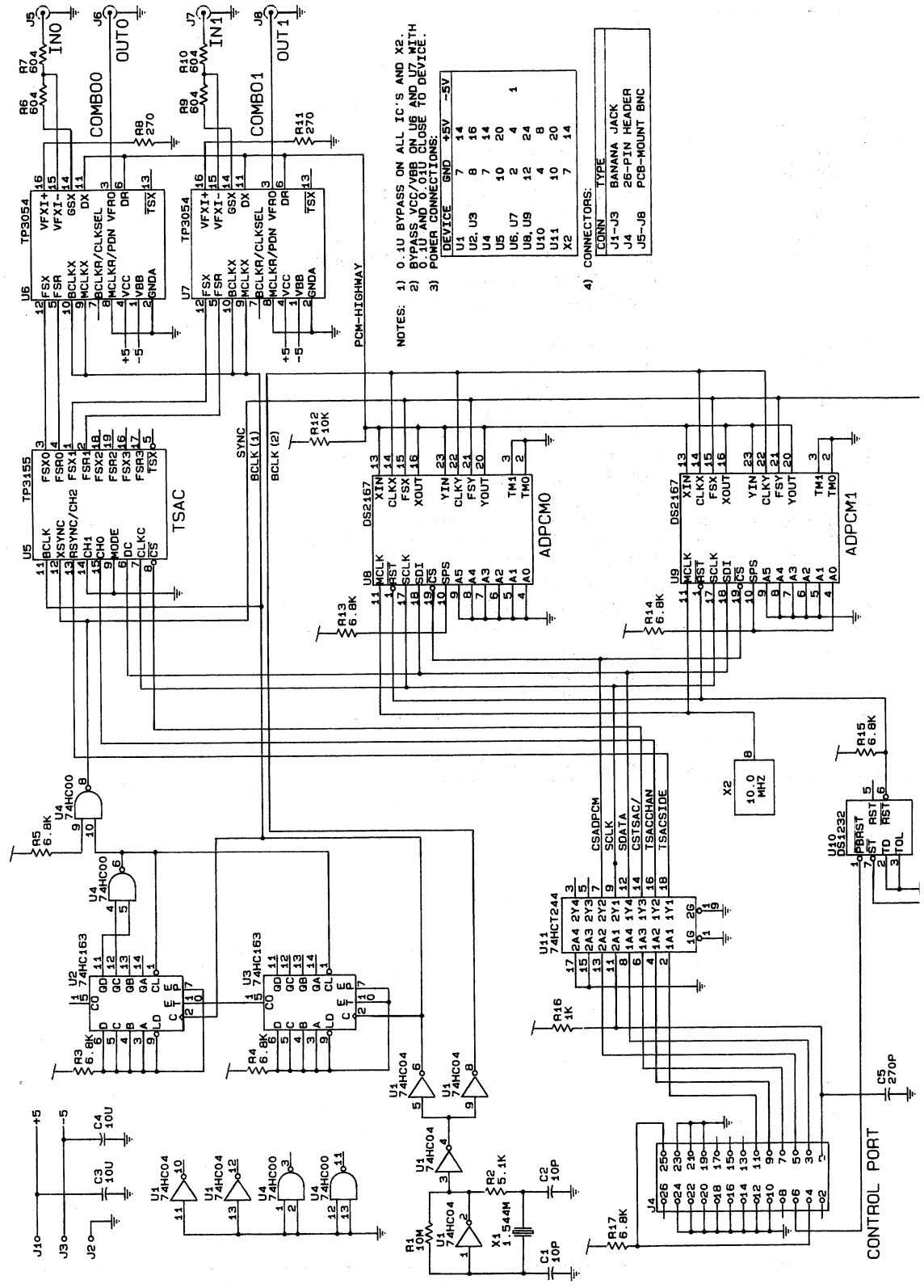lished with ease. No "glue" circuitry was required to do this—the Evaluation Board used but a few pull-up resistors and a port buffer for the DS2167s. The techniques demonstrated here extend to systems with as many as 64 DS2167s sharing common data and control lines. For applications which do not require this degree of flexibility, the DS2167's hardware mode alleviates the need for serial communication while maintaining the demonstrated performance.

Controller Program Command Summary	
Connection Selection Commands	
cursor up	Select connection above.
cursor down	Select connection below.
cursor left	Select connection to the left.
cursor right	Select connection to the right.
home	Select top-left connection.
end	Select bottom-right connection.
page up	Search up for another connection in this link.
page down	search down for another connection in this link.
Device Configuration Commands	
number	Set connection time slot to **number**.
u-Law	Select u-Law data format.
A-LaW	Select A-Law data format.
Compress	Select PCM-to-ADPCM compression mode.
Expand	Select ADPCM-to-PCM expansion mode.
Bypass	Select or toggle bypass mode.
Idle	Select device standby state.
Function Key Commands	
F1	Give help summary.
F2	Change display or port setup.
F3	Write configuration to board.
F4	Reset ADPCMs.
F5	Reset ADPCM algorithm for selected connection.
F6	Change ADPCM device address.
F7	Load configuration from file.
F8	Save configuration to file.
F9	DOS escape.
F10	Exit program.
Other Commands	
Control/L	Redraw screen.
Control/C	Exit program.

Evaluation Board Parts List	
U1	74HC04 Hex Inverter
U2-U3	74HC163 Binary Counter
U4	74HC00 Quad Two-Input NAND
U5	TP3155 Time Slot Assignment Circuit
U6-U7	TP3054 u-Law CODEC/Filter Combo
U8-U9	DS2167 (or DS2168) ADPCM Processor
U10	DS1232 Micromonitor
U11	74HCT244 Octal Buffer
C1-C2	10pF Capacitor
C3-C4	10uF Capacitor
C5	270pF Capacitor
(4)	0.01uF Capacitors (U6, U7 decoupling)
(14)	0.1uF Capacitors (U1-U11, X2 decoupling)
R1	10Mohm, ¼W, 5% Resistor
R2	5.1Kohm, ¼W, 5% Resistor
R3-R5, R13-R15	6.8Kohm, ¼W, 5% Resistor
R6, R7, R9, R10	604ohm, ¼W, 1% Resistor
R8, R11	270ohm, ¼W, 5% Resistor
R12	10Kohm, ¼W, 5% Resistor
R16	1Kohm, ¼W, 5% Resistor
J1-J3	Banana Jack
J4	26-pin Header Connector
J5-J8	BNC Connector
X1	1.544MHz Crystal
X2	10MHz Crystal Clock Oscillator

10

ADPCM EVALUATION BOARD

Dallas Semiconductor
T1 Design Kit

DS2180K

FEATURES

- Demonstrates key "hardware mode" attributes of the DS2180/DS2176 pair, such as:
  - Framing/synchronization
  - Link supervision and control
  - Signaling supervision
  - Rate adaption to equipment backplanes
- Expedites new designs by eliminating first-pass device prototyping
- Easily interfaced to user host controller for "software mode" evaluation
- User-supplied line interface allows direct connection to T1 lines
- Kit components include:
  - DS2180 T1 Transceiver
  - DS2176 T1 Receive Buffer
  - Printed circuit board
  - Support logic and clock generation circuitry
  - Applications and assembly information
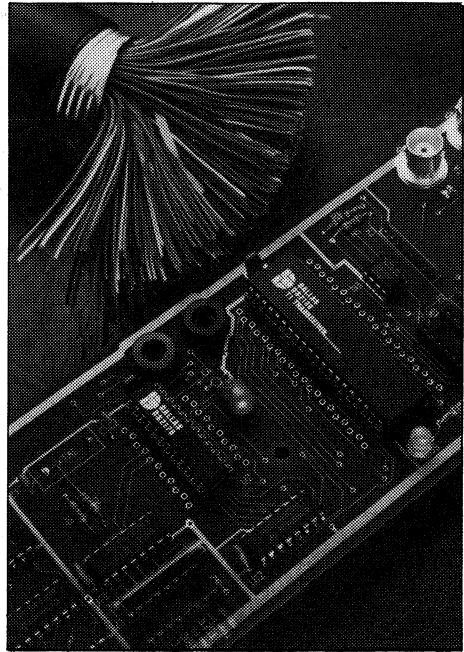
10

DESCRIPTION

The DS2180K allows the user to evaluate the performance of the DS2180 T1 Transceiver and DS2176 T1 Receive Buffer in an actual system environment. The evaluation board requires +5 volts; board inputs and outputs are TTL-compatible. Test points and control options on the board simplify selection of device feature sets required by the system designer.

Kit assembly requires approximately 1 hour. Although designed for hardware mode operation, a small wire-wrap area is provided for user-supplied host processor interface.

See Application Note 11 for further information.
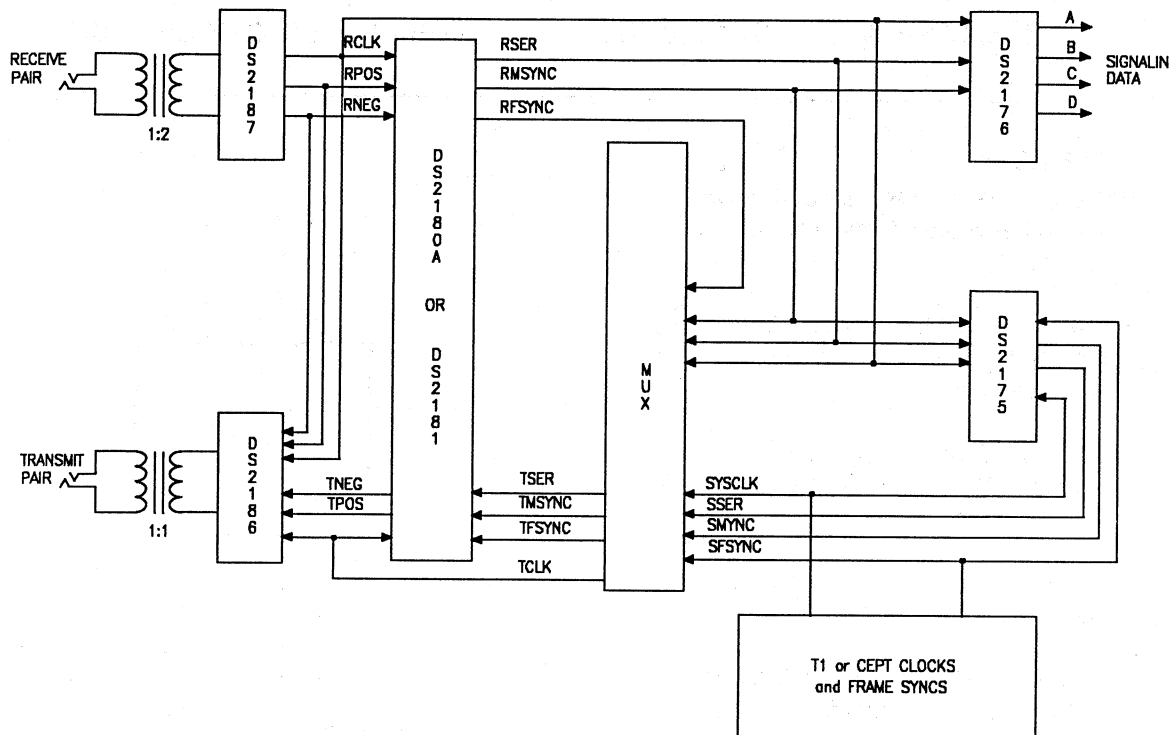
Dallas Semiconductor T1/CEPT Design Kit

FEATURES
- Demonstrates entire T1 and CEPT chip family

- Expedites new designs by eliminating first-pass prototyping

- Interfaces directly to IBM PC, XT, AT and compatibles through the parallel printer port

- High-level graphic software controls and monitors board functions

- Kit includes:
  - DS2180A or DS2181
  - DS2186
  - DS2187
  - DS2176
  - DS2175
  - Transmit and receive transformers
  - T1 (1.544 MHz) and CEPT (2.048 MHz) clocks and frame syncs
  - PC board with all necessary support logic
  - Documentation and control software diskette

- Transceiver works in the "software" mode

- Wire-wrap area and easy accessable test points allow customization to meet user's need

- Board comes completely assembled

DESCRIPTION
The DS2180DK and DS2181DK allow the user to evaluate the entire T1 or CEPT line card chip set. The design kits can be connected either to transmission test equipment or directly to T1 or CEPT lines. Received data can be run to a simulated backplane or can be looped back directly. The design kits operate off a single +5V supply. The controller program runs under MSDOS or IBM DOS version 2.0 or later.

## DS2180DK/DS2181DK BLOCK DIAGRAM Figure 1

Dallas Semiconductor
T1 NETWORK INTERFACE UNIT
DESIGN EVALUATION KIT

FEATURES

- Self-contained system for performance evaluation of the DS2190 Network Interface Unit

- Pre-assembled kit includes DS2190 NIU, DS2180A transceiver, transmit clock and data generator

- Connects directly to test equipment, including T1 frame generator, line simulator, jitter generator and analyzer

- Supports ESF and D4 framing, B8ZS and B7 stuffing

- On-board switches access all NIU mode options; LED indicators for system status, including synchronization loss and CRC errors; test points for additional critical signals

- Prototyping area for user customization

- Powered by single +5V supply
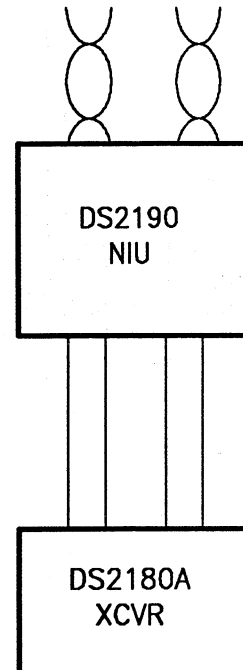
DESCRIPTION

The DS290DK contains all of the interface and framing functions required to connect to a simulated T1 communications line. The board is organized for easy control over and monitoring of the DS2190 operation. It is a helpful tool for evaluating the DS2190 in-system performance.

Additional circuitry may be easily added in the prototyping area to emulate the user's end application. An additional area contains a computer interface so that the DS2180A serial port may be accessed with user-developed software.

Dallas Semiconductor
MODEM Evaluation Kit

DS6151
DS6153

FEATURES

- IBM PC-based evaluation kit for DS6101/61103 Modems
- Two versions:
  - DS6151 supplied with DS6101 Modem
  - DS6153 supplied with DS6103 Voice Synthesis Modem
- Printed circuit board provides socket for Modem, RJ11 telephone jack and headset jack; plugs into expansion slot on IBM PC
- Supplied with headset
- Evaluation software on floppy disk
- Supplied with complete operating instructions
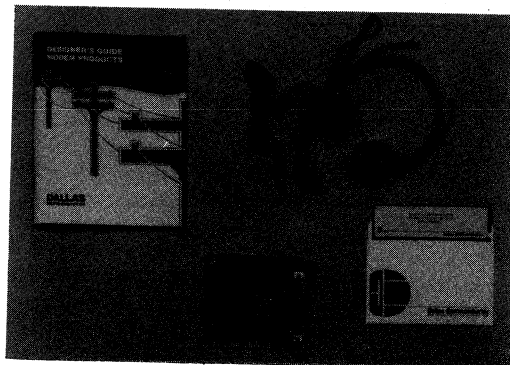
DESCRIPTION

The DS6151 and DS6153 Modem Evaluation Kits provide immediate evaluation of the DS6101 and DS6103 Modems. The kits supply all of the necessary hardware, software and documentation for use with an IBM PC. A printed circuit card which sockets the appropriate Modem plugs directly into the backplane of the PC and provides a modular RJ11 connector to a telephone line. In addition, a jack for the headset which is supplied with the kit is mounted on the board. A complete set of documentation with instalation and operating instructions is also supplied. A user need only have a private telephone line with a modular plug to insert into the RJ11 jack and he or she can be using the modem to converse in voice, transmit data or listen to synthesized voice responses in just a few minutes.

11

For more information on this product, see the Modem Designers Guide.

Application Notes

Dallas Semiconductor
T-Carrier Chip Set

Application Note-6

11

T-CARRIER CHIP SET ADAPTS TO CHANGING NETWORK STANDARDS

As T1 gains mainstream acceptance as the backbone of high-speed communications, ICs that meet the timing, control and compatibility demands of T1 electronics are becoming a necessity.

The interconnection of personal computers, terminals and telephones in the business environment is experiencing explosive growth. T1 is a cost effective means of linking such automated offices, and serves as an alternative to high speed modems in the data transport environment. T1 is a high-speed digital network (1.544 MHz) developed by AT&T in the early 1960s to support long-haul pulse-code modulation (PCM) voice transmission. Although twisted-pair copper wire is the primary transmission medium, multiple T1 networks are supported by optical fiber, microwave and satellite links. T1 (also known as DS1) is the primary interface between the local telephone operating companies and long distance carriers such as MCI, LDS and AT&T. The local operating companies also utilize T1 in subscriber line carrier systems (SLC-96) to connect remote subscribers to the central office.

As the development of support ICs for T1 networks becomes a crucial design issue, three major design challenges for T1 electronics have emerged: framing and synchronization, control and status monitoring and backplane compatibility. A new chip set from Dallas Semiconductor, which consists of the DS2180 Serial T1 Transceiver and DS2176 T1 Receive Buffer, addresses all three challenges. This chip set, implemented in low-power CMOS technology, is compatible with both North American and Far East T-carrier networks. It supports a wide variety of features, including D4 framing, extended framing, bipolar eight zero substitution (B8ZS) and total transparency zero suppression modes. In addition, the DS2180 eliminates the substantial off-board logic necessary to interface to system control circuitry.

STANDARDS AND SERVICES

Many large corporations have utilized leased T1 lines for point-to-point data networks. These lines are higher speed cousins of the traditional leased-line modem networks. The nonswitched networks are often incompatible with each other and with the Bell system equipment, and are becoming increasingly obsolete.

The competitive atmosphere generated by divestiture has reduced the cost of T1 connections and has accelerated the introduction of special data services based on T1. These new switched services require equipment compatible with Bell system equipment, and offer performance superior to leased-line alternatives. Customer controlled reconfiguration (CCR) is one such service in which cost is based on the percentage of link utilization. CCR is cost effective at data rates that use 20 to 25 percent of the available T1 bandwidth.

The existing T1 network must be upgraded to handle the demands of increasing data traffic. These upgrades include full data transparency and extended framing. Transparency eliminates the data corruption caused by existing signaling and zero suppression techniques. Extended framing provides the network with a 4-kbit data channel, which is used for alarm and error-rate monitoring. The data channel lets the network police itself, providing superior line-fault analysis.

T1 networks can also be used on-site as an alternative to LANs in the office environment. Currently, two computer-to-PABX interface specifications based on T1 technology exist. The Digital Multiplexed Interfaced (DMI) standard is supported by AT&T Information Systems and Hewlett-Packard. The Computer-Peripheral-Interface (CPI) standard is backed by Northern Telecom and Digital Equipment Corp. This widespread acceptance of T1 as a prime mover of voice and data is turning it into the "RS-232" of telecommunications.

Companies developing T-carrier equipment include those specializing in PCM switching and transmission, office automation, modem and communications networks and private automatic branch exchanges (PABX) with data capability.

FRAMING AND SYNCHRONIZATION

The first challenge in designing ICs for T1 is framing and synchronization. In the Dallas Semiconductor chip set, the DS2180 transceiver handles these functions. It supports extended framing, D4 framing and derivatives of D4, such as SLC-96. In addition, features such as bit 7 stuffing (a zero suppression technique), bipolar eight zero substitution (B8ZS) and total transparency zero suppression modes are included in the device. The transceiver has autonomous transmit and receive sides. An on-board serial port links the device to a host microprocessor/microcontroller for supervision and control.

The transmit side of the DS2180 is made up of six major functional blocks: a timing and clock generator, a yellow alarm circuit, an F-bit data section (F-bit refers to the first bit transmitted), a cyclic redundancy check (CRC) section and a data selector bipolar coder. The timing and clock-generation circuit develops all on-chip and output clocks from three signal inputs (TCLK, TFSYNC and TMSYNC). The output clocks identify robbed-bit signaling (which indicates the telephone on/off-hook status) and link-data frames, making them useful for data conditioning and decoding. The rising edge of the sync inputs must be aligned with the transmit clock. Data inputs are sampled on the falling edge of the clock signal, while updated outputs occur on the rising edge. The timing inputs on the transmit side may be slaved to receive side outputs for use in drop-and-insert applications. This timing sequence is compatible with most combo-codecs.

The yellow alarm circuitry generates mode-dependent alarms for transmission into the network. The F-bit data block develops the synchronization pattern that is embedded in the outgoing data stream. The CRC circuitry subsection produces check-sum codes that are utilized in extended framing. These three subsections feed into the data selector, which builds the outgoing serial data stream via bit selection and insertion. The bipolar coder reformats the data selector output into an alternative mark inversion (AMI) format and inserts the selected zero suppression techniques. The bipolar coder also supports an on-chip loopback feature.

The heart of the receiver is the synchronizer/ sync monitor, which monitors the incoming data stream for loss of frame or multiframe alignment, and searches for new alignment when synchronization loss is detected. The synchronizer uses a sophisticated, memory-intensive frame-search algorithm. Unlike earlier devices, this algorithm displays no sensitivities to emulators of the framing pattern sequence, such as digital milliwatt. It also rejects randomly induced patterns generated by network testing equipment that mimic synchronization patterns.

The Receive Control Register allows the user to tailor the characteristics of the sync algorithm to unique applications. Typical synchronization times are 4 ms (D4 framing) and 8 ms (extended framing). The resynchronization sequence occurs off-line. (The receive output timing "rolls" at the "old" alignment until the sync search is completed.) When the new frame and multiframe alignments are identified, the output timing set is jammed to the timing position of the next multi-frame boundary. When synchronization is established, the synchronizer is disabled to save power.

The output timing on the receive side is identical to the transmit timing; the bipolar decoder, yellow alarm detector and CRC circuitry are complements of those blocks used on the transmit side of the device. Alarm conditions detected on the receive side (loss of synchronization, carrier loss, framing error) appear as outputs and are reported to the status and error-count registers. The Receive Mark Register allows idle or digital milliwatt codes to be selectively inserted over incoming channels. This feature can be used in channel-unit applications for channel-level adjustment and field service.

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CONTROL AND STATUS MONITORING

A major disadvantage of most first-generation transceivers is that they require substantial off-board logic to interface to system control, or they support rigid control protocols which limit the host control options of the designer. The DS2180's on-board serial port utilizes a simple synchronous protocol and interfaces directly to popular microprocessors/microcontrollers, such as the 8051. Sixteen registers establish the device's operating characteristics and report error status and alarm conditions. This flexible control architecture eliminates support hardware and minimizes processor overhead.

The read/write timing for the port used to access the registers is independent of the transmit and receive timing. This read/write timing is compatible with the 8051 on-board serial port operating in mode 0. With a master clock of 12 MHz, the 8051 can write or read a single register in less than 25 us. In addition, a burst mode allows all registers to be consecutively read or written.

The basic operational control characteristics of the transceiver are established by the Common Control, Transmit Control and Receive Control Registers (CCR, TCR and RCR). The CCR establishes frame, zero suppression and yellow alarm modes. A local loopback, which internally ties the transmit clock and data outputs to the receive clock and data inputs, is also enabled by the CCR. The TCR supports blue (unframed "I's") and yellow alarm transmission. Robbed-bit signaling and D4 framing insertion modes are also selected by the TCR. The RCR establishes synchronizer characteristics and selects the code word type that may be inserted in each outgoing channel.

Three other register sets are used to eliminate the off-chip control hardware that is used in existing designs. The Transmit Idle Register (TIR) allows the user to insert an idle code sequence into any outgoing channel data. The Transmit Transparency Registers (TTR) are used to disable robbed-bit signaling insertion and bit seven zero suppression on a per-channel basis. The Receive Mark Regis-

ters (RMR) replace selected incoming DS0 channels with a digital milliwatt or idle code (as selected by the RCR).

Status monitoring is handled by the Receive Status Register, which reports alarm conditions, such as a loss of synchronization, yellow alarm, carrier loss, blue alarm and error-count saturation. Unless disabled by the Receive Mask Register, any one of these events will generate an interrupt. On-board error event counters allow the device to log error events, such as bipolar violations and frame bit errors. When the error counters exceed a preprogrammed threshold, they will also generate an interrupt (unless masked). This logging capability eliminates the need for off-chip error counting logic and minimizes processor overhead. Error-event service routines may be poll or interrupt-based, depending on the system requirements.

The DS2180 also has the ability to operate in hardware mode. For preliminary system prototyping or for applications which do not require serial port features, the transceiver may be reconfigured into a hardware mode. This disables the port, clears all internal registers and redefines all serial port pins as mode control inputs. This mode allows device retrofit into existing applications where mode control and alarm conditioning are performed with discrete logic. The mode control inputs establish device framing, zero suppression, alarm and F-bit insertion characteristics.

BACKPLANE COMPATIBILITY

The Dallas Semiconductor DS2176 T1 Receive Buffer is the first T-carrier product which lets the user link transceivers to a variety of system backplanes. The DS2176 compensates for jitter and wander in the receive clock, serves as a rate buffer for backplane frequencies other than 1.544 MHz, interfaces directly to serial or parallel backplanes and supervises robbed-bit signaling.

Although the received T1 data stream averages 1.544 MHz, the data displays significant high-frequency jitter and low-frequency wander. These characteristics result from

the less-than-perfect transmission charac-
teristics of a repeated T1 span line. An
elastic store, based on first-in, first-out
(FIFO) memories and discrete contention
logic, is required to interface transceivers to
system backplanes.

The DS2176 uses an on-chip PCM buffer to
synchronize incoming data to system back-
plane frequencies, eliminating the need for
the elastic store. The buffer depth is two
frames (386 bits), which is more than ade-
quate for most applications in which short-
term jitter and wander compensation is re-
quired. This buffer "slips" whenever it is
completely emptied or filled, recentering its
depth to one frame. (The buffer can also be
externally recentered.) Slip occurrences are
reported at the SLIP output. In addition, a set
of signals (System Multiframe Sync and Re-
ceive Multiframe Sync) can be used to moni-
tor buffer depth in real time.

SIGNALING SUPERVISION
Signaling data embedded in the PCM data
stream is extracted and output by the
DS2176. The signaling buffer in the DS2176
allows the device to freeze the signaling out-
puts during slip or alarm conditions. This
meets the Bell system requirements for pro-
hibiting updates when sync or carrier signals
are lost.

Signaling integration is another important
feature of the DS2176. When selected, it min-
imizes the impact of random noise on the
signaling information. For signaling integra-
tion, the channel signaling data must be in
the same state for two or more multiframes
before being updated at the signaling out-
puts. For the DS2176, two inputs are used to
select the degree of integration or totally by-
pass the feature. The processed signaling
data is not re-merged with the outgoing chan-
nel word. This maintains data integrity in
mixed voice-data or data-only environments.

A T1 TUTORIAL
T1 transmission is based on twisted pair wir-
ing, with separate pairs used for the transmit
and receive sides. T1 links require a repeater
circuit every 6,000 feet to regenerate the at-
tenuated signal; an "office repeater" is re-
quired when a loop terminates into station
electronics. Higher rate transmission sys-
tems based on optical fibers are gaining
widespread use. DS3 is one such system; at
45 MHz, it is made up of 28 T1 (DS1) lines.

In T1, data is transmitted in an alternate
mark inversion (AMI) format, which allows
clock signals to be derived from data, elimi-
nating the need for separate clock transmis-
sion. The clock signal is extracted from the
AMI waveform using phase-locked loops or
LC tank circuitry. Clock extraction circuitry
requires a minimum density of "1's" to oper-
ate correctly. To meet this density require-
ment—networks cannot transmit a code
consisting solely of zeros—existing T-carrier
equipment changes bit 7 of any channel con-
sisting solely of "0's" to 1. Bit 7 stuffing
does not affect the quality of voice transmis-
sion, but it does corrupt data significantly.
An alternative to bit 7 stuffing is bipolar
eight zero substitution (B8ZS), which
replaces any transmitted zero octet with a
B8ZS code word. If the last "1" transmitted
was positive, the inserted word is 000 + -0- + .
If the last "1" transmitted was negative, the
code word inserted is 000 - + 0 + - . Bipolar vio-
lations occur in the fourth and seventh bit
positions, but these are ignored by the re-
ceive alarm circuitry when B8ZS is enabled.
The receive side detects the code word and
replaces it with all zeros.

Framing refers to the format for data signal-
ing, alarm and synchronization information
on the T1 trunk. A frame of data is made up
of 193 bits, and is transmitted every 125 us.
The first bit transmitted is known as the
F-bit. The F-bit position is used for syn-
chronization, alarm and network data link.
The F-bit is followed by 24 voice or data
channels, each channel being eight bits
wide. These channels (known as DS0 chan-
nels) each have a data rate of 64 kbits/s.

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Multiple frames make up a superframe (multiframe). One Extended Superframe consists of 24 frames. Twelve frames make up one D4 superframe.

Signaling information (telephone on-hook/off-hook status, known as robbed-bit signaling) is written over the least significant bit (LSB) of each channel every six frames. Newer systems avoid this type of data corruption by moving all signaling information to a separate DS0 channel. The use of common-channel signaling and newer zero suppression techniques such as B8ZS enhance the network's ability to carry data. This capability is known as "clear channel."■

DS2180DK/DS2181DK
Potential users of the Dallas Semiconductor T1/CEPT Chip Set may wish to purchase a DS2180DK or DS2181DK demo kit.

Dallas Semiconductor
DS2180 Supervisory Software

Application Note-7

11

INTERFACING THE DS2180 T1 TRANSCEIVER TO 8051/31 MICROCONTROLLERS

This application note provides users of the DS2180 T1 Transceiver with some 8051 software examples. All of the software presented makes use of the serial control port of the DS2180, which allows access to 16 internal registers devoted to device control, configuration and status monitoring. The serial port consists of 5 pins: SDI, SDO (serial data in and out), SCLK (serial data clock in), $\overline{CS}$ (chip select) and $\overline{INT}$ (interrupt output). Although the port is very general-purpose, this application note concentrates on interfacing specifically with an 8051 processor. When configured in mode 0, the serial port of the 8051 mates perfectly with the serial port of the DS2180, requiring no external logic. This circuit hook-up is shown in Figure 1.

Circuit operation is very straightforward. RXD on the 8051 is a bi-directional serial bus for data in and out of the part. The TXD pin provides a serial data clock to the DS2180, allowing the transceiver to sample data on rising clock edges. A normal port pin (P1.0) enables the DS2180's port by transitioning low. The remaining connection, INT0, processes interrupt requests from the DS2180's $\overline{INT}$ output. Because this output is open-collector, a resistor pull-up is necessary to define the high state. Use of the $\overline{INT}$ output is strictly up to the user and usually depends on whether processor control is polled or interrupt-based.

Speed through the port can be very rapid and is determined by the processor internal clock. For example, if the 8051 is running at 12 MHz, then the serial clock output at TXD will be i MHz (a $\div$ 12 of the master clock), which leads to typical read/write times of less than 25 $u$sec. Because of the $\overline{CS}$ input, several DS2180s can be supervised by the same processor by tying the clock and data lines together, and selecting each DS2180 by its $\overline{CS}$ input.

The first two software examples concentrate on how to transfer data between the 8051 and the DS2180 using the serial port. Both methods of transfer—burst and random—are supported. (Burst mode means all registers are accessed consecutively, while random mode means accessing one specific register.) The third and last example shows how DS2180-generated interrupts might be handled, specifically those interrupts caused by on-chip counter saturations. This software is useful when the user is building code to calculate BERs (bit-error-rate) for bipolar violations, CRC-6 checksum errors, loss-of-sync occurrences (OOFs) etc. Note that the software using the DS2180 internal counters obsoletes the need for external error count logic, reducing board area and cost.

Finally, this software is not meant to be a stand-alone program: it simply illustrates subroutines that may be incorporated into a larger program.

DS2180/8051 SUGGESTED HOOK-UP
Figure 1
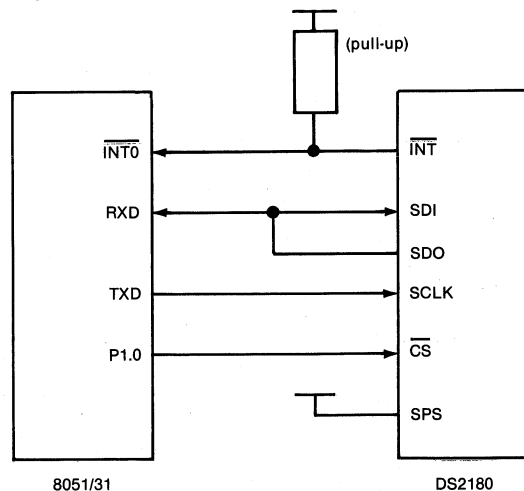
SERIAL PORT READ ROUTINES Example 1
Purpose: Read registers from the 2180 via the serial port

Arguments: Burst mode
        R0 Count of bytes to receive (16)
    DPTR External memory location

            Random Access mode
      R1 T1 register address (0-15)
    ACC Data returned from DS2180

```
;
; Process burst read request
;
T1__BURST__READ:    PUSH        DPL             ;save data pointer low
                    PUSH        DPH             ;save data pointer high
                    MOV         R1,#81H         ;burst read command byte
                    SJMP        T1__RD          ;begin serial byte transfer

;
T1__RANDOM__READ:   PUSH        DPL             ;save data pointer low
                    PUSH        DPH             ;save data pointer high
                    MOV         R0,#1H          ;only 1 byte to transfer
                    MOV         DPTR,#FFFFH     ;point to dummy location
                    XCH         A,R1            ;get the T1 reg address
                    ANL         A,#0F           ;mask out invalid bits
                    RL          A               ;shift left one bit
                    ORL         A,#1H           ;indicate a read function
                    XCH         A,R1            ;....and save the result

;
; Begin reading data from the serial port (RXD, TXD)
;
T1__RD:             SETB        P1.0            ;disable DS2180
                    CLR         P1.0            ;enable DS2180
                    PUT__SERIAL__PORT R1 (write command byte)

;
T1__RLP:            GET__SERIAL__PORT A (read data byte)
                    MOVX        @DPTR,A         ;store this byte
                    INC         DPTR            ;point to next destination byte
                    DJNZ        R0,T1__RLP      ;continue until all reg done
                    SETB        P1.0            ;set DS2180 CS pin high
                    RET                         ;return to caller
```

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MACRO DEFINITIONS

```
.MACRO          PUT__SERIAL__PORT    REG
                CLR     SCON.REN        ;disable serial receive
                CLR     SCON.T1         ;clear transmit done flag
                MOV     SBUF, REG       ;write serial byte
        LBL1:   JNB     SCON.T1,LBL1    ;wait until transfer complete
                CLR     SCON.T1         ;clear transmit done flag

.MACRO          GET__SERIAL__PORT    REG
                SETB    SCON.REN        ;enable serial receive
                CLR     SCON.R1         ;read serial byte
        LBL2:   JNB     SCON.R1,LBL2    ;wait until transfer complete
                MOV     REG,SBUF        ;fetch the byte just read
                CLR     SCON.REN        ;disable serial receive
```

SERIAL PORT WRITE ROUTINES Example 2
Purpose: Write registers to the 2180 via the serial port

Arguments: Burst mode
    RO Count of bytes to transmit (16)
    DPTR External memory location

        Random Access mode
    R1 T1 register address (0-15)
    ACC Data value for transfer

```
;
; Process burst write request
;
T1__BURST__WRITE:   PUSH    DPL         ;save data pointer low
                    PUSH    DPH         ;save data pointer high
                    PUSH    ACC         ;save caller's accumulator
                    MOV     R1,#80H     ;burst mode command byte
                    MOVX    A,@DPTR     ;get first data byte
                    SJMP    T1__WT      ;begin actual transfer

;
' Process random write request
;
T1__RANDOM__WRITE:  PUSH    DPL         ;save data pointer low
                    PUSH    DPH         ;save data pointer high
                    PUSH    ACC         ;save caller's accumulator
                    MOV     R0,#1H      ;only 1 byte to transfer
                    MOV     DPTR,#FFFFH ;point to dummy location
                    XCH     A,R1        ;retrieve DS2180 address
                    ANL     A,#0FH      ;mask out invalid bits
                    RL      A           ;shift left 1 bit
                    XCH     A,R1        ;....and save the result
```

```
;
; Begin writing data out to the serial port
;
T1__WT:          SETB       P1.0                  ;disable DS2180
                 CLR        P1.0                  ;enable DS2180
                 PUT__SERIAL__PORT R1 (write command byte)
;
T1__WLP:         PUT__SERIAL__PORT A (write data byte)
                 INC        DPTR                  ;point to next byte
                 MOVX       @DPTR,A               ;store this byte
                 DJNZ       R0,T1__WLP            ;continue until all reg done
                 SETB       P1.0                  ;disable DS2180
                 RET                              ;return to caller
```

SOFTWARE FOR PROCESSING COUNTER-GENERATED INTERRUPTS FROM THE DS2180 Example 3

This routine processes interrupts on the INT0 line (Pin 12 of the 8051), generated by the $\overline{INT}$ output of the DS2180. In general any alarm bit set in the receive status register (RSR) will cause the $\overline{INT}$ pin to go low if the corresponding bit in the receive interrupt mask register (RIMR) is also set. This software example responds to interrupts generated by either a BVCS (bipolar count saturation) or an ECS (error count saturation) event. While the BVC counter is a full 8-bit counter, the ECR consists of two separate 4-bit counters in the same register. The high nibble increments on loss-of-sync occurrences and the low nibble increments on F-bit errors (the type of F-bit errors are mode-dependent). Saturation of either 4-bit counter will set the ECS bit in the RSR register.

Program flow is as follows: when an interrupt occurs, the RSR register is read to determine which counter saturated. The memory location mapping to the appropriate saturated counter is then incremented to keep a running tab of saturation occurrences. The counter in question is reloaded with a user-determined threshold before the routine returns control to the main program. This routine assumes that RIMR.7 and RIMR.6 have already been set high to allow counter-generated interrupts to occur.

```
;
; Define the external memory addresses used by this routine
;
T1__BVC__RELOAD = #0H                             ;bipolar count threshold
T1__ECR__RELOAD = #1H                             ;error count threshold
T1__BVC__ERRORS = #2H                             ;bipolar sat count
T1__ESF__ERRORS = #3H                             ;low nibble ECR sat count
T1__OOF__ERRORS = #4H                             ;high nibble ECR sat count
;
; Read the T1 receive status register (RCR)
;
ERRCHK:     MOV      R1,#T1__RSR                  ;load register address
            LCALL    T1__RANDOM__READ             ;read one T1 register
            JB       A.7,BVCS                     ;process bipolar count sat
            JB       A.6,ECS                      ;process error count sat
            SJMP     INTO__R                      ;....or terminate interrupt
```

```
;
; Process a bipolar violation count saturation by first reloading the user-defined count thresh-
; old and then incrementing the running count memory location (T1__BVC__ERRORS).
;
BVCS:       MOV         DPTR,#T1__BVC__RELOAD
            MOVX        A,@DPTR                     ;fetch BVC count threshold
            MOV         R1,#T1__BVCR                ;fetch BVCR address
            LCALL       T1__RANDOM__WRITE           ;write one T1 register
            MOV         DPTR,#T1__BVC__ERRORS
            MOVX        A,@DPTR                     ;fetch running count
            INC         A                           ;increment count by 1
            MOVX        @DPTR,A                      ;put new count back
;
; Now check for any other counter saturation
;
            SJMP        ERRCHK
;
; Process error count saturation by a similar procedure except that we must determine which
; nibble of the ECR is affected. Then only the counter saturated is reset to the user-specified
; value.
;
ECS:        MOV         R1,#T1__ECR                 ;load register address
            LCALL       T1__RANDOM__READ            ;read one T1 register
            MOV         R0,A                        ;store ECR count in R0
            ANL         A,#0FH                      ;mask to get low nibble
            XRL         A,#0FH                      ;xor to see if saturated
            JNZ         ECS__OOF                    ;if not, must be high nibble
            MOV         A,R0                        ;restore ECR count
            ANL         A,#F0H                      ;mask to save high nibble
            MOV         R0,A                        ;save high nibble
            MOV         DPTR,#T1__ECR__RELOAD
            MOVX        A,#DPTR                     ;get ERC threshold value
            ANL         A,#0FH                      ;mask to get low nibble
            ORL         A,R0                        ;or high and low nibbles
            MOV         R0,A                        ;save as new ERC count
;
; Now increment the low nibble (T1__ESF__ERRORS) running count
;
            MOV         DPTR,#T1__ESF__ERRORS
            MOVX        A,@DPTR                     ;fetch ESF running count
            INC         A                           ;increment count by 1
            MOVX        @DPTR,A                      ;put new count back
```

```
;
; Now check for high nibble (OOF counter) saturation and process this event similarly.
;
ECS_OOF: MOV      A,R0                      ;restore ECR count value
         ANL      A,#F0H                    ;mask to get OOF count
         XRL      A,#F0H                    ;xor to see if saturated
         JNZ      ERRCHK                    ;if not, then we are done
         MOV      A,R0                      ;restore ECR count value
         ANL      A,#0FH                    ;mask to save low nibble
         MOV      R0,A                      ;save low nibble
         MOV      DPTR,#T1_ECR_RELOAD
         MOVX     A,@DPTR                   ;get ECR threshold values
         ANL      A,#F0H                    ;mask to save high nibble
         ORL      A,R0                      ;or high and low nibble
         MOV      R0,A                      ;save as new ECR count
         MOV      DPTR,#T1_OOF_ERRORS
         MOVX     A,@DPTR                   ;get OOF running count
         INC      A                         ;....and increment by 1
         MOVX     @DPTR,A                   ;put new count back
;
; Finally, write new value of ECR back into the T1 (DS2180) Transceiver.
;
ECS_WT:  MOV      A,R0                      ;transfer new count to ACC
         MOV      R1,#T1_ECR                ;load T1 ECR address
         LCALL    T1_RANDOM_WRITE           ;write one T1 register
INTO_R   RET                               ;return to main program
```

Dallas Semiconductor
T1 Demo Kit

Application Note 11

11

DS2180/DS2176 T1 DEMO KIT

This application note describes the Dallas Semiconductor DS2180/DS2176 T1 demonstration kit. The DS2180 T1 Transceiver is a single-chip CMOS device that integrates all the digital control circuitry necessary for supervising T1 lines operating at 1.544 Mbits/sec. The DS2176 Receive Buffer is a companion part (also CMOS) that integrates the elastic store and robbed-bit signaling buffer functions typically required for a T1 line card. Used together, they provide an optimum, efficient solution for complicated T1 interface problems.

T1 KIT CONTENTS

The kit contains a printed-circuit board which permits easy evaluation of the DS2180/DS2176 parts. On-board circuitry generates all the different timing necessary for operation of the t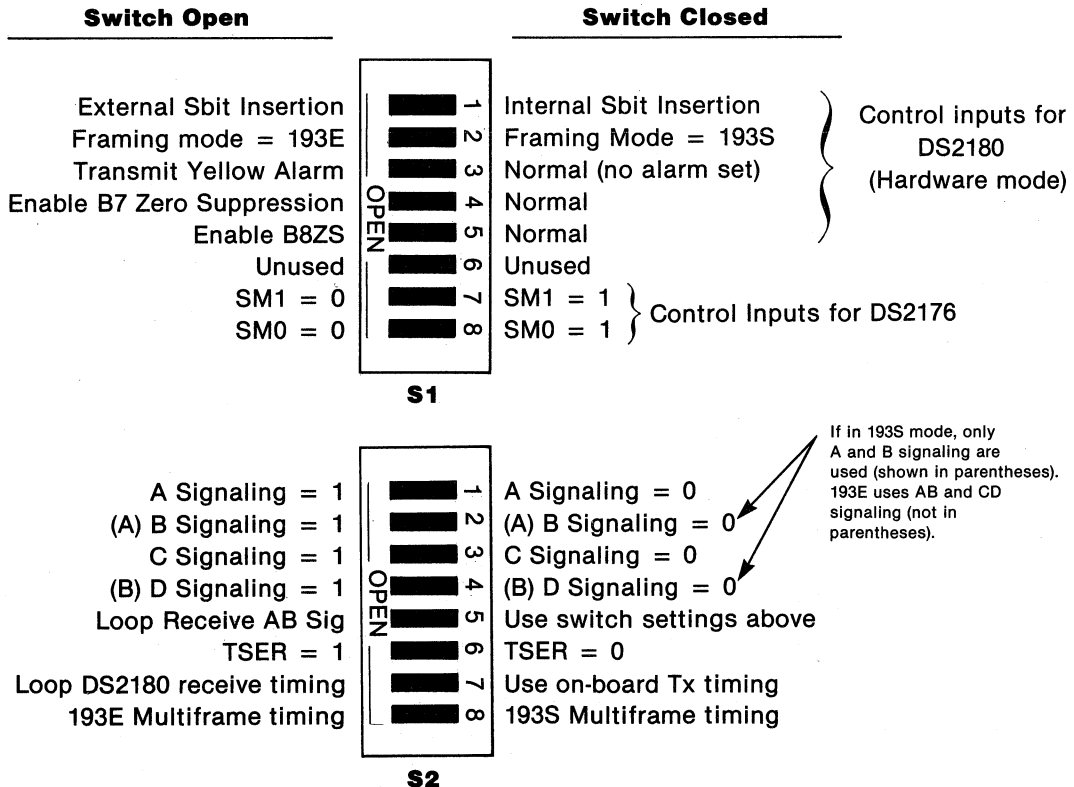ransmit side of the DS2180. The user also has the ability to insert ABCD robbed-bit signaling into the transmit T1 data stream and/or to loop the receive-side timing and data to the transmit-side of the DS2180 for emulating drop-and-insert applications.

The kit also includes a 1.544 MHz crystal, resistor pull-ups, HCMOS logic parts, the DS1231 Power Monitor and, of course, samples of the DS2180 and DS2176. Remaining components may be obtained from a local electronics distributor. The parts list for these items appears at the back of this document.

PCB DESCRIPTION

The PCB contains the digital logic necessary for generating transmit timing and for multiplexing internal signals. Two banks of switches are used for selecting operating modes, signaling states, and timing configuration.

Figure 1 **BOARD SWITCH SETTINGS**

Switch Open		Switch Closed	
External Sbit Insertion	1	Internal Sbit Insertion	⎫
Framing mode = 193E	2	Framing Mode = 193S	Control inputs for DS2180
Transmit Yellow Alarm	3	Normal (no alarm set)	(Hardware mode)
Enable B7 Zero Suppression	4	Normal	
Enable B8ZS	5	Normal	⎭
Unused	6	Unused	
SM1 = 0	7	SM1 = 1	⎱ Control Inputs for DS2176
SM0 = 0	8	SM0 = 1	⎰

S1

Switch Open		Switch Closed	
A Signaling = 1	1	A Signaling = 0	
(A) B Signaling = 1	2	(A) B Signaling = 0	If in 193S mode, only A and B signaling are used (shown in parentheses). 193E uses AB and CD signaling (not in parentheses).
C Signaling = 1	3	C Signaling = 0	
(B) D Signaling = 1	4	(B) D Signaling = 0	
Loop Receive AB Sig	5	Use switch settings above	
TSER = 1	6	TSER = 0	
Loop DS2180 receive timing	7	Use on-board Tx timing	
193E Multiframe timing	8	193S Multiframe timing	

S2

Holes in the board are intended for the user to insert banana plugs for VDD and GND and BNC connectors for unipolar NRZ data and clock. For adding additional circuitry (such as a line interface), a small wire-wrap area is provided.

In order to stuff the board, silkscreening shows the locations of all the components specified in the parts list. Brief mnemonics on the switch locations should help in selecting options; however, a full switch explanation is shown in Figure 1 and can also be inferred from the board schematic shown in Figure 2. Although not numbered, decoupling capacitors on all ICs are recommended and their locations are outlined on the board, usually at the top of the IC (near Pin 1).

TRANSMIT TIMING AND DATA

The master clock for transmit is generated by a 1.544 MHz Pierce crystal oscillator whose buffered output is available at U8-6 (Pin 6). From this clock the frame and multiframe sync pulses are derived. Frame sync is a one-clock-wide pulse with a frequency of 8 KHz. Multiframe sync is also a one-clock-wide pulse but with a period of either 12- or 24-frame sync pulses, depending upon the state of switch S2-8 (193E/193S). 12-frames-per-multiframe is used in D4 systems while 24-frames-per-multiframe is used in the emerging ESF format. *It is important that this selection be compatible with the DS2180 framing mode selected by switch S1-2.*

U12 is a multiplexor chip that determines which timing set is fed to the DS2180 transmit sync inputs (TMSYNC, TFSYNC, TCLK): either the normal crystal-derived timing mentioned above or the receive-side output timing signals of the DS2180. Also selected is the data origin for transmit data into the DS2180 (TSER): either switch S2-6 or looped from the receive data output of the DS2180 (RSER).

Please note that the transmit frame and multiframe pulses are not required by the DS2180 and are only included on the board to allow testing of all possible timing applications. In fact, by tying the TMSYNC and TFSYNC input low, the internal counters will derive both of these signals. (The internal multiframe sync will be indicated by TMO.) Please refer to the DS2180 data sheet for full details on transmit timing operation.

TRANSMIT SIGNALING INSERTION

Robbed-bit signaling is input to the DS2180 at Pin TABCD and comes from the output of U13, another multiplexer chip. 4- or 16-state signaling (AB in D4 mode and ABCD in ESF mode) can be programmed by S2-1 through S2-4. Alternately, the user may loop receive-side buffered AB signaling from the DS2176 into the TABCD input. (Looping of 16-state signaling is not supported on the board.) S2-5 (RABCD/MAN SIG) determines which signaling configuration is selected.

DS2180 OPERATING MODES

If switch S1 is used on the demo board, it will configure the DS2180 transceiver in the hardware mode, where operating modes are selected by tying pins high or low. This is in contrast to the DS2180's serial-port mode whereby a serial port interface allows access to internal registers that determine those same operating modes as well as many others. Tying the SPS pin (Pin 19) low selects the hardware mode, while tying it high activates the serial-port interface. Note on the schematic that using S1 automatically ties SPS low.

To evaluate the serial port operation of the DS2180, the user may use a 16-pin header connected via a ribbon cable to his software development station. The header would then fit into the socket vacated by S1. The required pinout for header is shown in Figure 3 and is also implied on the schematic. Note that power and ground are assumed to origi-

Figure 3
SERIAL PORT HEADER PINOUT (S1)
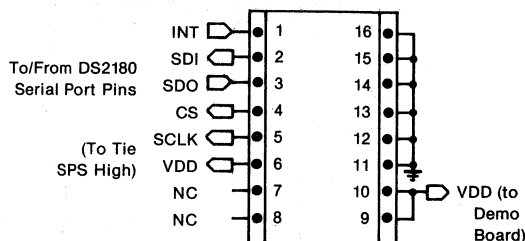
Pinout shows assignment of port signals when S1 is not used and ribbon cable header is connected from User Development Station.

Figure 2 **DS2180/DS2176 DEMO BOARD SCHEMATIC**

nate from the development station instead of the banana plugs. Power is required on Pin 6 of the header in order to tie SPS high. The low-pass filter formed by R5 and C3 may be necessary to minimize excessive under-shoot and ringing caused by long ribbon cables. Please refer to the DS2180 data sheet for a full explanation of the serial port interface and its required timing.

DS2180 INTERFACE FORMAT

Transmit and receive data can be handled in two different ways on the demo board. For applications using the NRZ unipolar format, data and clock can be supplied to and from the BNC connectors. To use the BNC con-nector path for RCV DATA, jumper pads J1 and J2 must be strapped together. However, in order to interface to bipolar digital data, some solder pads are provided for accessing the bipolar inputs and outputs of the DS2180. The transmit bipolar pads are TPOS and TNEG while the receive bipolar inputs are RPOS and RNEG.

Clocking for transmit data out is available at either the BNC connector or the solder pad labeled TCLK. Data present at TPOS and TNEG or at the BNC connector is updated on rising edges of transmit TCLK. Receive data present at either the RCV DATA connector or at the bipolar inputs is sampled by falling edges of RCV CLOCK (or RCLK if using the solder pad).

DS2180 SYNC INDICATOR

When the DS2180 is in a resync mode, search-ing for the framing pattern, the RLOS pin will go high. This will illuminate L1, a small red LED. When the part has established proper sync, RLOS will return low and the LED will go out.

DS1231 POWER MONITOR/POWER-ON RESET

Initialization of the DS2180 is accomplished by tying the $\overline{RST}$ input low for some brief time when power is first applied. The DS1231 per-forms this task and also monitors power for voltage glitches that a simple RC network would otherwise miss. Power-on reset for the DS1231 nominally lasts 500 msec, during which time the DS2180 will be out-of-sync.

DS2176 OPERATION

The main job of the DS2176 is to synchronize the incoming T1 line frequency to the system data clock. Long-term differences in fre-quency are resolved by the use of controlled slips, whereby a frame of data is either de-leted or repeated. On the demo board, the T1 clock line is RCLK and the system clock is the crystal-derived transmit clock. Slip oc-currences can be monitored at the SLIP pin on the DS2176.

By default on the board, the DS2176 receive buffer is configured in the serial data (S/$\overline{P}$ = 1) and the 1.544 MHz system clock modes (SCLKSEL = 0). However, the type of signal-ing buffer configuration can be changed by use of switches S1-7 and S1-8 (which tie SM0 and SM1 high or low). Please consult the DS2176 data sheet for details on proper selection for your application.

TEST POINTS

Surrounding both the DS2180 and the DS2176 are open pads in which small test pins may be soldered for conveniently attaching scope probes.

PARTS LIST FOR DS2180/2176 DEMO BOARD

	ITEM #	P/N	DESCRIPTION	QTY
*	U1	DS2180	Single-chip T1 transceiver	1
*	U2	DS2176	T1 Receive buffer	1
*	U3	DS1231	Power monitor/Power-on reset circuit	1
*	U4-U7	HC163	4-Bit presettable counters	4
*	U8, U9	HC04	Hex inverters	2
*	U10	HC00	Quad 2-input NAND gates	1
*	U11	HC02	Quad 2-input NOR gates	1
*	U12	HC257	Quad 2-input data selector/multiplexer	1
*	U13	HC251	8-input data selector/multiplexer	1
*	XTAL	MP-2	M-TRON 1.544 MHz crystal	1
	R1	—	5KΩ resistor, 5%	1
	R2	—	10 Meg, 5%	1
	R3	—	330Ω, 5%	1
	R4	—	1KΩ, 5%	1
	R5	—	220Ω, 5%	1
*	Z1	710A104	Allen-Bradley SIP resistor packs (10), 100KΩ	1
*	Z2, Z3	708A104	Allen-Bradley SIP resistor packs (8), 100KΩ	2
	C1-C3	—	10 pF capacitors, 10%	3
	C4	—	10 uF decoupling capacitor	1
	C5	—	0.1 uF decoupling capacitors (on all ICs)	13
	S1, S2	76SB08	Grayhill rocker DIP switches	2
	L1	—	Red LED	1

* Indicates parts are shipped with T1 Demo Kit.

SLC-96 SYSTEM BLOCK DIAGRAM Figure 1
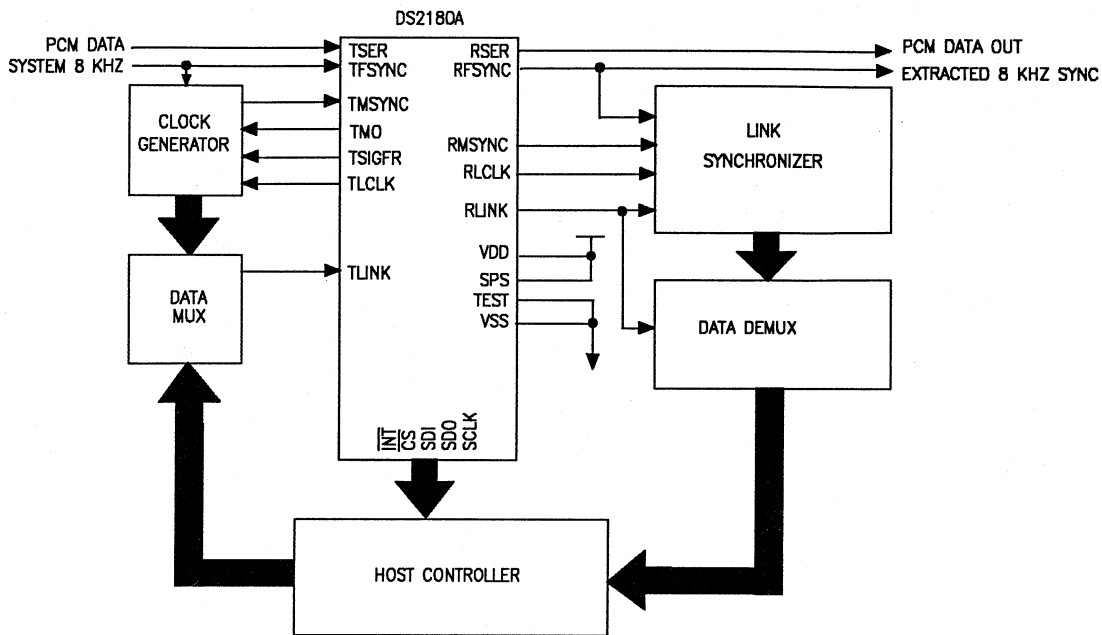
NOTES:
1. This simplified block diagram does not show all DS2180A I/O; it indicates only one of several control options available to the SLC-96 system designer.

Dallas Semiconductor
DS2180A Based SLC-96 System

Application Note 16

DS2180A BASED SLC-96 SYSTEM

SLC-96 is a T1 based digital Subscriber Loop Carrier system developed by AT & T which utilizes a modified D4 framing format on 1 (or more) of 4 T1 lines in a 96 subscriber configuration. The system periodically "steals" the Fs framing bit position present in D4 framing and replaces it with a low speed data link. A SLC data link frame is 9 ms in length and is made up of 6 D4 multiframes. Please refer to the DS2180 data sheet for details of D4 (193S) framing.

The 36 Fs bit positions in the SLC data link frame include a "normal" 12 bit Fs reframe pattern (00011100111) and a 24-bit data link pattern. The 24 bits of the data link pattern are aranged as follows:

CONCENTRATION FIELD (C-FIELD)
　　　- bits 1 thru 11
SPOILER (FIXED 010 PATTERN)
　　　- bits 12 thru 14
MAINTENANCE FIELD (M-FIELD)
　　　- bits 15 thru 17
ALARM DATA LINK FIELD (A-FIELD)
　　　- bits 18 thru 19
PROTECTION LINE SWITCH FIELD (S-FIELD)
　　　- bits 20 thru 23
SPOILER FIELD (FIXED 1 PATTERN)
　　　- bit 24

The spoiler bits are used to "align" the data link timing with the multiframe timing established by the reframe pattern. See Bell Core document TR-TSY-000008 for more details.

TRANSMIT DATA LINK

Off-chip logic must be combined with the DS2180A to support the transmit side data link. D4 framing (CCR.4 = 0) and external Fs bit insertion (TCR.2 = 1) must be selected on the DS2180A. A user designed mux "steers" the resync pattern or appropriate data link information to the TLINK input. TLINK will sample the mux output during every Fs bit period. The resync pattern is the exclusive NOR of outputs TMO and TSIGFR and serves as one input to the mux. Other mux inputs may include shift registers and/ or latches written by a host processor. The data

mux is driven by a clock generator circuit whose outputs are logical combinations of TMO, TLCLK and TSIGFR. The clock generator also establishes multiframe boundries by pulsing TMSYNC once per data link frame.

MULTIFRAME SYNCHRONIZATION

The receive synchronizer of the DS2180A must be programmed to Ft/Fs cross coupling (RCR.3 = 1) and minimum sync time (RCR.2 = 0). This allows the device to "frame-up" immediately to the resync field as it appears at the receive data inputs. Under these conditions worst case reframe time is approximately 10 ms. Other synchronizer options require a longer valid Fs pattern and will not frame to SLC-96. The "errored" Fs patterns caused by the data link will be reported at RFER and logged in the error event counter, they will not cause an auto-resync (the auto-resync feature - RCR.1 = 0 - reacts to Ft errors only.)

Disabling auto-resync (RCR.1 = 1) allows the user to establish his/her own resync criteria. The resync criteria may be determined by the link synchronizer described below. The user may also change the sync criteria (RCR.1 = 0) after sync is declared to eliminate the false Fs error reporting at RFER and in the error event counter. RCR.1 must be set to 1 prior to the next resync command (RCR.0 = 1) or synchronization will never occur.

DATA LINK SYNCHRONIZATION/LINK DATA DEMUX

Synchronization to the SLC data link must be performed off-chip. RLINK, RLCLK and RMSYNC are the only transceiver outputs required to feed the user designed link synchronizer. Link synchronizer outputs alert host control if link synchronization is lost. The host will respond by commanding the DS2180A and/or the link synchronizer to resync.

The link synchronizer also outputs decode clocks which drive a data demultiplexer. The demux circuitry extracts incoming link data from the RLINK output and interfaces to host control.

DS2180A BASED DROP AND INSERT SYSTEM Figure 2
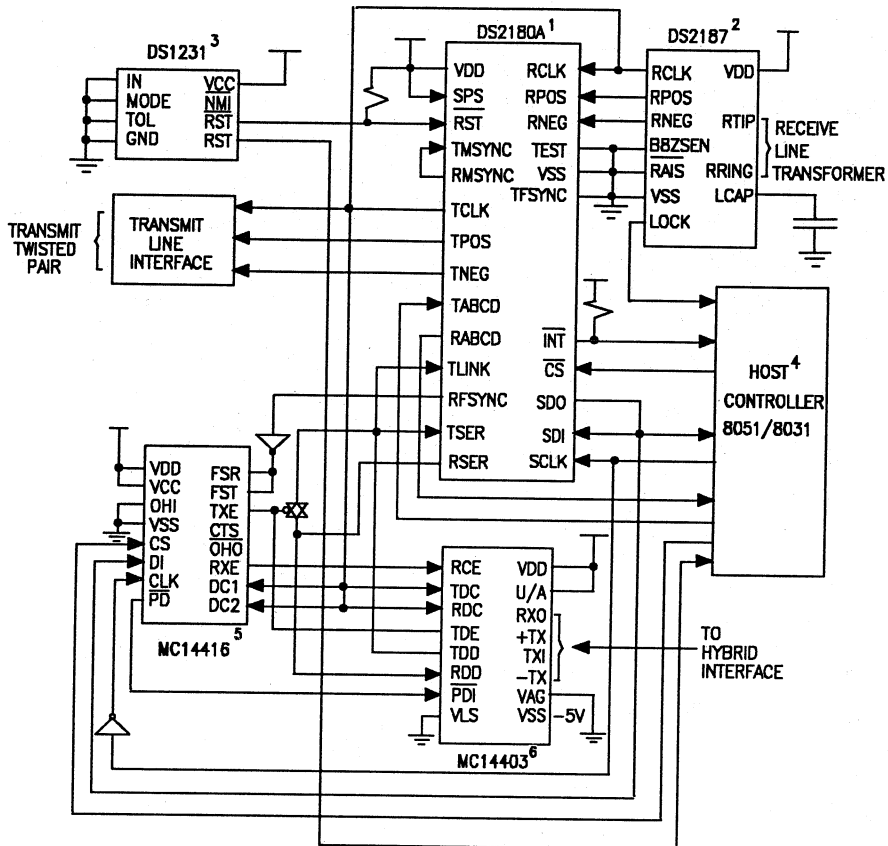
NOTES:

1. The timing set of the DS2180A Transceiver allows the transmit side inputs to be "slaved" to receive side outputs.

2. The DS2187 T1 Receive Line Interface extracts clock and data with no off-chip precision components.

3. The DS1231 Micromonitor monitors Vcc level and provides power-on reset pulses to the DS2180 and host controller.

4. Dallas Semiconductor application note #7 ("DS2180 Supervisory Software") - Provides control programming examples utilizing the 8051/8031 family of microprocessors.

5. MC14416 Motorola Timeslot Assignment Circuit (TSAC) - Identifies DSO channel to be dropped and inserted. Programmed via host controller's serial port.

6. MC14403 Motorola combo codec - Other combo vendors with compatible products include National, Intel, and Hitachi.

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